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A Final Report for:

SILICON-BASED LIGHT-EMITTING DIODES

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ATTN: Richard O. Ulsh
P.O. Box 12211
Research Triangle Park, NC
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The views, opinions and/or findings contained in this report are those the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

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One Patriots Park
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13. ABSTRACT *(Maximum 200 words)*

We have demonstrated the fabrication of heterojunction porous silicon visible light-emitting devices (LEDs). Our device consists of a heterojunction between electrochemically etched p-type porous silicon and indium-tin-oxide (ITO), a transparent n-type semiconductor which was deposited by sputtering. On the basis of three independent measurements, current-brightness, current-voltage, and current-temperature, our results indicate that observed electroluminescence (EL) originates from minority (electron) carrier injection, the basic mechanism operating in GaAs-based LEDs or other homojunction devices. Our finding indicates that EL should be possible with the same impressive efficiency levels as the photoluminescence (PL) which was observed for porous silicon.

However, the quantum efficiency of present devices has been compromised because the contacting areas between wide bandgap materials and porous Si are only a very small portion of the total porous Si surface. Present techniques used for LED fabrication only provide a contact to the tip of the pores; therefore, most of the surface of the light-emitting porous Si region is inactive in EL. Conformal coverage of a transparent conductive wide bandgap material into porous Si would enhance the quantum efficiency. Atomic layer epitaxy (ALE) growth of GaN (side-wall epitaxy), or electroplating of a transparent conducting oxide could increase the contact area which would result in an enhancement of EL efficiency.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (continued)

LIST OF FIGURES (concluded)

LIST OF TABLES

PROJECT SUMMARY

We have demonstrated the fabrication of heterojunction porous silicon visible light-emitting devices (LEDs). Our device consists of a heterojunction between electrochemically etched p-type porous silicon and indium-tin-oxide (ITO), a transparent n-type semiconductor which was deposited by RF sputtering. We have also carried out a study to determine electrical properties and structural characteristics of these porous silicon/ITO structures. On the basis of three independent measurements, current-brightness, current-voltage, and current-temperature, our results indicate that observed electroluminescence (EL) originates from minority (electron) carrier injection, the basic mechanism operating in GaAs-based LEDs or other homojunction devices. Our finding indicates that EL should be possible with the same impressive efficiency levels as the photoluminescence (PL) which was observed for porous silicon. Furthermore, no fundamental principles have been observed which would otherwise limit the efficiency of emissions of these devices.

However, the quantum efficiency of present devices has been compromised because the contacting areas between wide bandgap materials and porous Si are only a very small portion of the total porous Si surface. Sputtering or e-beam evaporation techniques, used for LED fabrication, only provide a contact to the tip of the pores, therefore, most of the surface of the light-emitting porous Si region is inactive in EL. A process which could result in conformal coverage of a transparent conductive wide bandgap material into porous Si would enhance the quantum efficiency to the impressive efficiency levels observed from porous Si with a liquid junction. For example, atomic layer epitaxy (ALE) growth of GaN (side-wall epitaxy), or electroplating of a transparent conducting oxide could increase the contact area which would result in an enhancement of EL efficiency. Use of transparent conducting polymers in principal results in an enhancement in light efficiency. However, at the present time, these devices suffer from a lack of stability.

1 INTRODUCTION AND BACKGROUND

Silicon is the basic building block for most electronic integrated circuits, but present interconnects between high speed silicon integrated circuits in computer systems remain the exclusive domain of low speed, large area nests of copper wiring, while the associated displays which serve as the interface to human operators usually depend on bulky cathode ray tubes. The present work addresses the formation of surface-emitting visible light-emitting diodes (SEVLED) in silicon allow chip-to-chip, board-to-board, and system-to-human information transfer in an extremely efficient manner by optical means, so that the silicon devices for emission, detection, and display of the information are monolithically integrated directly into the silicon wafers themselves. Silicon light-emitting devices and silicon photovoltaic detectors, embedded in each integrated circuit, will allow extremely rapid transfer of data within the processor. Emission wavelengths throughout the visible spectrum may be achieved with this work, allowing that flat panel optical displays necessary for transferring the information from computer systems to human operators will also be manifested entirely in silicon.

1.1 Problems to be Solved and the Deficiencies of the Existing Technology

The need for developing optical communications technology between chips and boards in high speed data processing equipment is well known. Present systems rely exclusively on copper wiring to provide circuit interconnects. This dependence on low speed copper wiring is creating massive bottlenecks at both the chip and the board level: VLSI chips are approaching the 500-1000 wire-bonded pin level, and typical boards contain over 300 chips leading to tens of thousands of wires. Optical interconnects offer the promise of alleviating these problems by providing serial rather than parallel data transfer at very high rates, with low power consumption, no rf interference problems, and high reliability. However, before this new technology can be effectively implemented, cost efficient fabrication processes must be realized, and simple methods for packaging the structures must be provided. Most current work is concentrated on providing hybrid approaches for utilizing standard GaAs light-emitters in the environment of VLSI, which is otherwise entirely based on silicon. However, the most promising III-V light-emitting compounds, such as GaAs and AlGaAs, are not readily deposited directly onto silicon substrates due to lattice and thermal expansion mismatches. These materials compatibility problems generally serve to degrade the performance of III-V compound light-emitting devices grown onto silicon. Another approach involves fastening GaAs-type devices onto the surface of the silicon wafer, either with solder or with glue: this is a costly, time consuming, labor intensive process. In addition, the interface between the computer and a human operator is in most cases accomplished with a massive cathode ray tube. Again, GaAs and its alloys offer the promise of light-weight, polychrome flat panel displays, but these compound semiconductors are generally found to be far too expensive for use as large area video display panels. Low cost visible light emitters based solely on silicon technology could solve all of the problems.

Unfortunately, standard crystalline silicon is not a good candidate for emitting light. Although crystalline silicon has excellent properties for use as electronic amplifiers and switches ("transistors"), and junction diodes which feature minority-carrier injection are readily demonstrated, its optoelectronic properties are severely compromised, because the material possesses an indirect optical band gap. In other words, in order for an electron in the excited state (conduction band) to recombine with radiative emission into the ground state (valence band),

a third body, *viz.*, a phonon, must be involved, and such three-body processes have extremely low probability. Specifically, for any light-emitting diode, the radiative recombination rate is found to be proportional to the product $B(\Delta n)p$, where Δn is the concentration of injected minority-carriers, p represents the majority-carriers, and B is a material specific constant. For example, $B = 7.2 \times 10^{-10}$ cm^3/s for direct gap GaAs, but only 1.8×10^{-15} cm^3/s for the indirect gap in silicon.[1] Thus although luminescence in the near infrared at 1.1 eV (1100 nm) can indeed be observed in standard silicon samples, it is extremely weak.[2] Undoubtedly, if a process could be developed that allowed efficient light emission to be obtained directly from the surface of the silicon chip itself, then a simple, low-cost method would be available for implementing optical interconnects and optical displays, and all other processes presently being pursued would be superseded.

In this context, it has recently been reported[3] that efficient light emission is indeed possible from silicon, if it the material is properly prepared in a microporous form, typically by electrochemical and/or chemical etching. As a direct consequence of the etch procedure, such porous silicon samples contain microscopic protuberances formed as a myriad of clusters located all over a porous sponge-like surface. High magnification transmission electron microscopy (TEM) appears to confirm that the surfaces mainly consist of almost one-dimensional structures, 10 nm or less in diameter.[4] Such nanostructures may be expected to exhibit quantum confinement effects, leading to a large increase in the effective energy gap.[5] In fact, the absorption edge for such "wires" with roughly a 20Å diameter was shown to be shifted to a wavelength of about 550 nm, which is in the yellow-green part of the spectrum.[5] Also, Halimaoui *et al*[6] have formed liquid junction devices using aqueous HCl or KNO_3 solutions to inject electronic carriers into porous silicon films, although the red light emission for these devices only lasted a few minutes, due to oxidation reactions.

This program has demonstrated[7,8] the successful fabrication of the first porous silicon-based np heterojunction LEDs. These devices were configured as heterojunctions between an n-type transparent indium-tin-oxide (ITO) layer and a p-type porous Si layer (PSL) exhibiting quantum confinement effects. Figure 1 shows a schematic and measured electroluminescence (EL) spectrum of these devices. We will present a discussion of the techniques for the fabrication of such devices herein, and also present the methods to increase light efficiency of porous Si LEDs. Our results have been confirmed by other researchers.[9,10]

1.2 Introduction to Porous Si

Porous silicon is usually prepared by the electrochemical dissolution of wafers of single crystal silicon,[11] although similar results can be obtained by starting with polycrystalline silicon films.[12] The structure of the resulting porous material depends on the conductivity type and the carrier concentration that characterizes the starting silicon wafer. In all cases, electrons must be removed from the liquid-solid interface, so that elemental silicon may enter the solution as either Si^{+2} or Si^{+4} ions. Bulk silicon wafers will not become etched in hydrofluoric acid without the presence of an external bias which can supply electronic holes.[13] Under the action of an applied positive bias, bonding electrons are removed from silicon atoms that are in contact with the electrolyte, and more rapid reaction rates appear to occur at certain local inhomogeneities. "Pores" therefore become etched into the surface. These pores continue to propagate into the bulk of the wafer, leaving silicon material behind in certain characteristic structures. A silicon

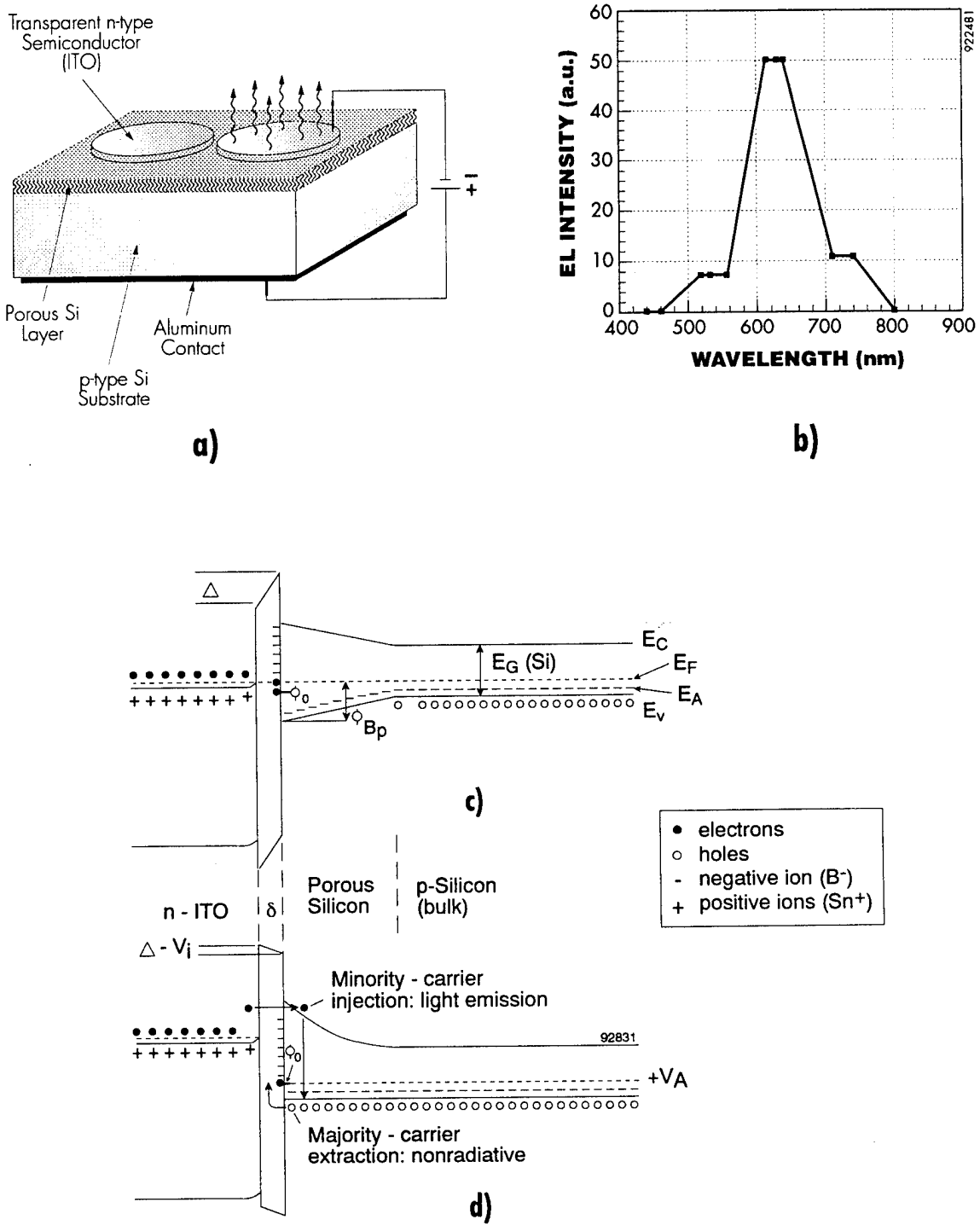


Figure 1 *An np heterojunction porous silicon LED capable of emitting light at visible wavelengths: a) schematic cross section; b) EL spectrum; c) band diagram model indicating stored charges and pathways in equilibrium; and d) in forward bias.*

morphology may form which in many respects resembles the dendrites that propagate under certain circumstances in front of an interface during the electrodeposition of metals from solution.[14] Alternatively, the porous silicon may resemble a sponge or coral. We must consider four cases which depend directly on the type of doping in the starting substrate: n-type or p-type, with either low doping range or degenerate doping levels.

P-type, Heavily Doped - It has been determined that a typical structure is formed with heavily doped p-type silicon wafers, corresponding to resistivities less than about 0.01 ohm-cm, or carrier concentrations exceeding about 10^{19} cm^{-3}.[15] Here electrons can be removed from atoms at the silicon-liquid interface via the valence band of the silicon, and the current transport through the wafer may be described in terms of a current of electronic holes. The overall chemical reaction is controlled by electrons tunnelling through a relatively narrow potential barrier between the electrolyte and the silicon. Because there exists a large concentration of holes in the valence band of the silicon, a large current is able to pass with a very small bias voltage (less than a volt). There are large densities of long, straight pores with a few branches, with normal crystalline silicon remaining between the pores. Therefore with heavily doped p-type silicon, long silicon "wires" are formed. Pore diameters tend to be in the range of 60 to 120Å or greater, with remaining silicon "wires" of roughly the same dimensions.[16] This material exhibits an electron diffraction pattern identical to bulk crystalline silicon.[17] If such "coarse" porous silicon is removed from the substrate, it shows the same gray color and basically the same absorption edge as bulk silicon.[5]

P-type, Lightly Doped - Once again, electrons can be removed from the silicon-liquid interface via the valence band. However, instead of long, straight pores, now a sponge-like structure is formed. Apparently, the hemispherical tip of a pore is basically unstable, and many new smaller pores can develop along its curved surface. Such new pores propagate in various directions, often intersecting other branching pores. Consequently, an overall random structure of silicon particles, all interconnected, remains as the reaction front propagates forward. The pore size in lightly p-type material tends to be smaller, roughly 25 to 50Å,[16] and the remaining silicon structures no longer present the diffraction patterns of perfect crystalline silicon,[17] instead showing a smearing of the patterns. This material possesses small enough dimensions to exhibit quantum confinement effects.

Smith, Chuang, and Collins presented a theoretical model for the formation morphologies of porous silicon based on the diffusion of a rate limiting specie, such as an electronic hole, to the liquid-silicon interface.[18] They assume that there is some type of "diffusion length" for holes, but the holes are majority-carriers: the only distance which Smith et al could correlate with a "diffusion length" was the width of a depletion region in the silicon at the surface with the solution. Although indeed we must expect a depletion region to be present with no bias applied, the etching is actually performed under forward bias conditions, which will shrink or even eliminate any depletion region. However, the current of holes must actually drift to the surface under the influence of the applied field. Etching is performed at roughly the same current level, 10 to 100 mA/cm^{-2}, regardless of doping concentration: with materials having low concentrations of free carriers, these carriers must be moving at higher velocities, to maintain the same level of current. For high resistivity material, a significant potential drop will occur across the wafer, due to the series resistance effect when the carrier concentration is low. Clearly, the drifting holes can acquire energy from the field, and arrive at the surface as hot holes. If several

hot holes should each impinge simultaneously at different positions on the circumference of a pore, then each can contribute to the chemical reaction because they possess energy acquired from the field. Consequently, each hot hole can cause a new pore to develop. Alternative models based on thermionic emission across a potential barrier suffer because under forward bias, the depletion region will be reduced or eliminated.

This model can explain the branching found in the pore structure of non-degenerately doped silicon. On the contrary, in heavily doped material, motion of holes is sluggish, they basically acquire no energy from the field, and the reaction occurs uniformly around the circumference of the pore, with the pore propagating straight forward with a relatively wide diameter. This difference in morphology due to carrier concentration effects has a profound influence on the light-emitting properties of the silicon structure.

N-type, Heavily Doped - Once again, in order to demonstrate etching, it is necessary to remove electrons from the chemically active surface. With n-type material, this can only be accomplished via the conduction band. Therefore, a reverse bias must be applied, which means placing a positive voltage on the rear contact of the wafer. Depending on how heavily doped the wafer is, reverse breakdown can occur with just a few volts applied, and a porous structure can be formed. With degenerately doped n-type material, a coarse structure exhibiting long pores in the direction of current flow is found, similar to heavily doped p-type material.

N-type, Lightly Doped - In lightly n-type silicon, a very large reverse bias, exceeding 10 volts, must be applied in order to break down the liquid-solid junction and allow electrons to enter the silicon conduction band. Such high electric fields make a very unstable interface, and etching is totally nonuniform. Thus material etched under these conditions is generally not useful.

However, one can etch lightly doped n-type silicon in the presence of light.[19] The light creates minority-carrier holes, which then allow electrons to leave the interface via the valence band. Very low biases, equivalent to p-type samples, are sufficient to allow etching to occur. n-type material etched under illumination turns out to be equivalent to lightly doped p-type porous silicon, with a sponge-like morphology.

1.3 Light Emission from Porous Silicon

Photoluminescence in the visible was reported for silicon nanostructures before light-emitting diodes were demonstrated. Generally, photoluminescence is a necessary but not a sufficient condition for electroluminescence, because problems with electrical contacts may prevent luminescence which depends upon the injection of minority-carriers. Let us briefly summarize photoluminescence in porous silicon.

Apparently the first report of visible light emission from sub-microscopic silicon particles was given by Takagi et al,[20] who produced silicon particles by means of microwave plasma decomposition of silane. The average crystallite size was 45Å, with a range of 25 to 140Å, embedded in a matrix of amorphous silicon. Upon oxidation of the mass of material to convert the amorphous silicon into SiO_2, smaller diameters were observed for the remaining silicon particles, and visible photoluminescence was observed. No light emission was observed from

crystallites with diameters larger than 60Å. It is clear that electrochemical reactions are not a prerequisite for preparing visibly luminescent silicon.

The first report of visible photoluminescence from electrochemically produced porous silicon was given by Canham, who attributed the light emission to quantum size effects.[3] This program has reported red, orange, yellow and green photoluminescence from different samples of porous silicon, depending on the etching conditions.[7] The emission data is shown in Figure 2. A vast literature on all aspects of photoluminescence in porous silicon has appeared in the last four years. Because photoluminescence is a prerequisite for electroluminescence, the general trend in photoluminescence data, directly applicable to electroluminescence. Based on the work done on this program[7] and that of Koshida[21] may be summarized as follows.

1. Porous silicon films formed on either n or p-type degenerately doped wafers do not exhibit visible photoluminescence.

2. Non-degenerately doped n-type samples only show visible photoluminescence if prepared under illumination.

3. The photoluminescence spectra show a blue shift as the current density during the electrochemical etching is increased. Note the different sizes of the particles may form at 25 mA/cm^2 and 200 mA/cm^2.[22]

4. The photoluminescence spectra show a blue shift with increasing substrate resistivity. This would be consistent with our model of the action of hot holes on contributing to interfacial breakdown.

5. If porous silicon samples are left for extended periods of time in solutions of fluoride ions without further biasing, the photoluminescence will become blue-shifted.

1.4 Injection Luminescence

The external quantum efficiency of forward bias injection luminescence at 1100 nm in conventional diffused crystalline silicon np junctions is less than 10^{-4}%, due to an indirect bandgap.[2] In contrast, the external quantum efficiency of direct bandgap GaAs light-emitting diodes exceeds 1%.[23] In the 1950s, visible electroluminescence was reported from silicon pn junction diodes subjected to a reverse bias;[24,25] the broad-band emission was white in color, and the generally accepted model invoked the relaxation of hot electrons in the conduction band. The efficiency of such devices proved to be too low to allow any commercial products to succeed. Thus, prior to the announcement of light-emitting porous silicon, there was no viable silicon light emitting device.

Electrochemical Injection Luminescence - The first report of bright visible light emission from porous silicon involved contact with an electrolytic solution. It was reported that if porous silicon samples are placed in simple aqueous electrolytes that do not contain any fluorine ions, then visible electroluminescence can be observed under electrical bias. Halimaoui et al[6] have formed liquid junction devices using aqueous HCl or KNO_3 solutions to inject electronic carriers

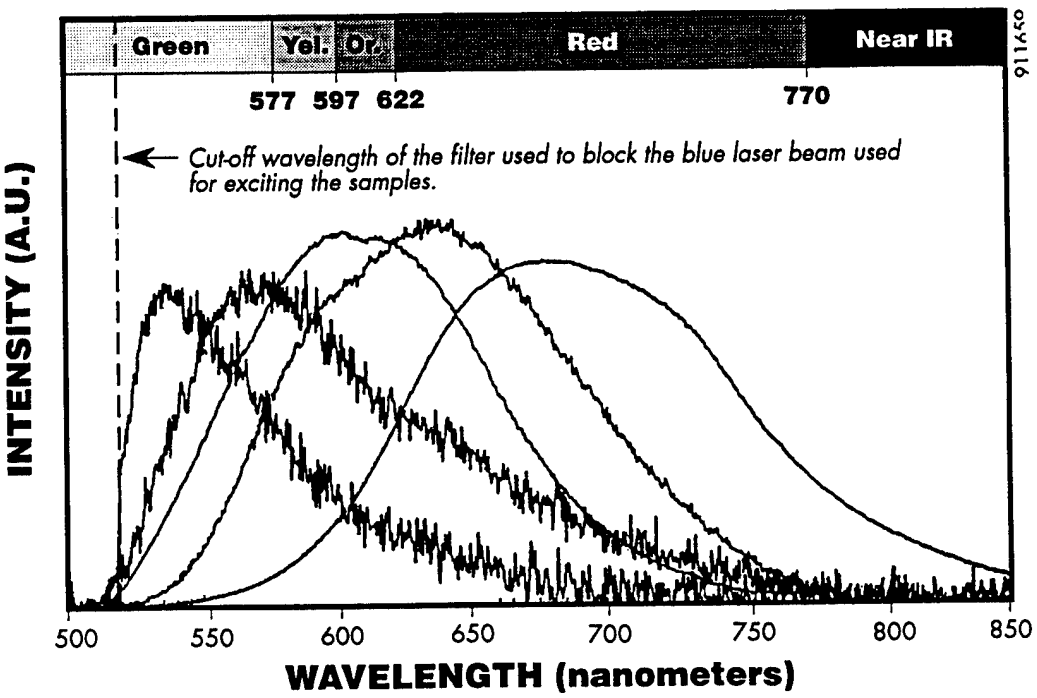


Figure 2 *Photoluminescence spectra of several porous silicon samples; excitation obtained with argon ion laser emitting at 488 nm. Note that emission at shorter wavelengths is weaker and more unstable over time.*

into porous silicon films, although the bright red light emission only lasted a few minutes, due to oxidation reactions. It was clear that under the conditions used, a film of SiO_2 formed all over the surface, impeding the flow of current. Electrical to optical conversion efficiencies exceeding 0.01% have now been observed.[26,27] Beale et al[28] described the depth dependence of both electroluminescence and photoluminescence for porous silicon samples held in an aqueous electrolyte (1M H_2SO_4 + 0.1M $Na_2S_2O_8$). Most important, they observed that for a p-type wafer with about 15 μm of porous silicon, both the electroluminescence and the photoluminescence were emitted from the entire thickness of the sample. Such electrolytic electroluminescence is quite bright, easily seen in a well lit room, but unfortunately unstable. However, it indicates that if a proper solid state contact can be made to porous silicon, bright injection luminescence should be obtained.

Solid State Injection luminescence - In the following we will summarize the EL results performed by other researchers using solid state contacts.

Richter et al,[29] reported EL from n-type silicon etched under illumination, with gold contacts sputtered onto the surface of the porous layer. Red light emission was observed with 200 volts applied, regardless of the polarity of the bias. In 1992 Koshida reported electroluminescence from porous silicon devices with rectifying characteristics.[30] They used non-degenerately doped p-type silicon wafers to form porous films 3 to 7 μm thick, with both gold and indium-tin oxide (ITO) contact pads on the surface. They presented a model based on

double injection of both electrons and holes into the porous silicon, with subsequent radiative recombination of the carriers. Futagi *et al*[31] relied on low doping density p-type silicon substrates, while forming an injecting contact with microcrystalline SiC. Under forward bias of about 24 volts, the device current suddenly increased dramatically to over 600 mA, and bright orange light, visible in a fully illuminated room, was observed. Steiner et al[32] have reported blue and green electroluminescence with porous silicon. They used low doping density n-type wafers and used ultraviolet illumination during the electrochemical etching procedure. They claim that UV illumination creates minority-carrier holes even in quantum confined particles, leading to continued dissolution to smaller sizes. Again we caution that this requires control of the removal of single layers of silicon to achieve a desired thickness, and furthermore, UV would continue to generate holes no matter how thin the silicon became, so all of the material should have dissolved, if hole generation is the controlling mechanism.

Finally, Steiner et al[33] have created a novel porous silicon device with the highest conversion efficiency (0.01%) ever reported. They started with lightly doped n-type silicon, and grew heavily p-doped silicon on the surface. During etching, the p-type material maintained the characteristics of standard silicon, forming a relatively large diameter wire structure. However, due to illumination during the etch, the n-type layer below the p-type layer developed the required nanoporous morphology. With a p-type silicon top contact, holes are readily injected into the porous material; electrons can be injected from the substrate. There are no heterogeneous materials present, as occurs with metal or ITO contacts. Although this structure is extremely promising, it still suffered from series resistance effects.

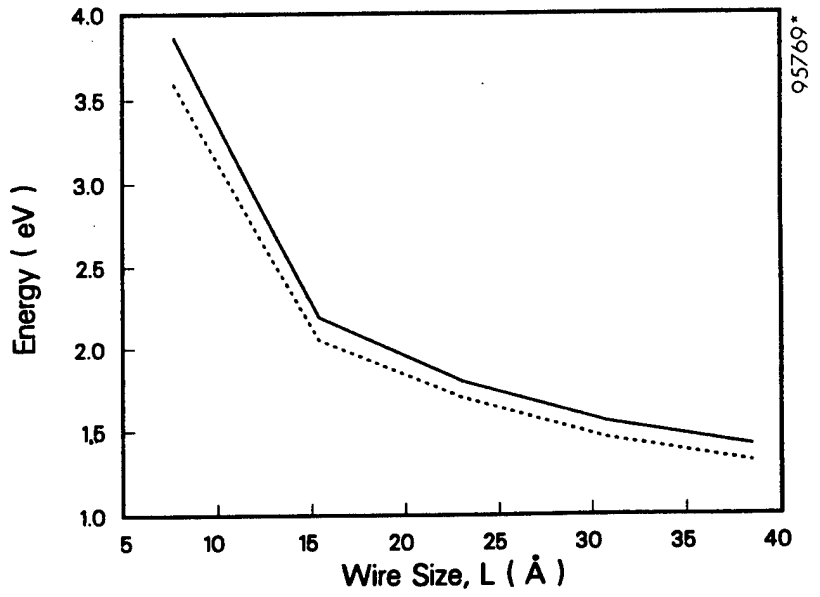
1.5 Quantum Confinement Effects

Theoretical Considerations - There appears to be a general consensus the very small physical sizes that are present in the etched silicon wire segments can lead to quantum confinement effects. The simplest picture is based on a particle in a box, from basic quantum mechanics theories. The confinement energy is given by,

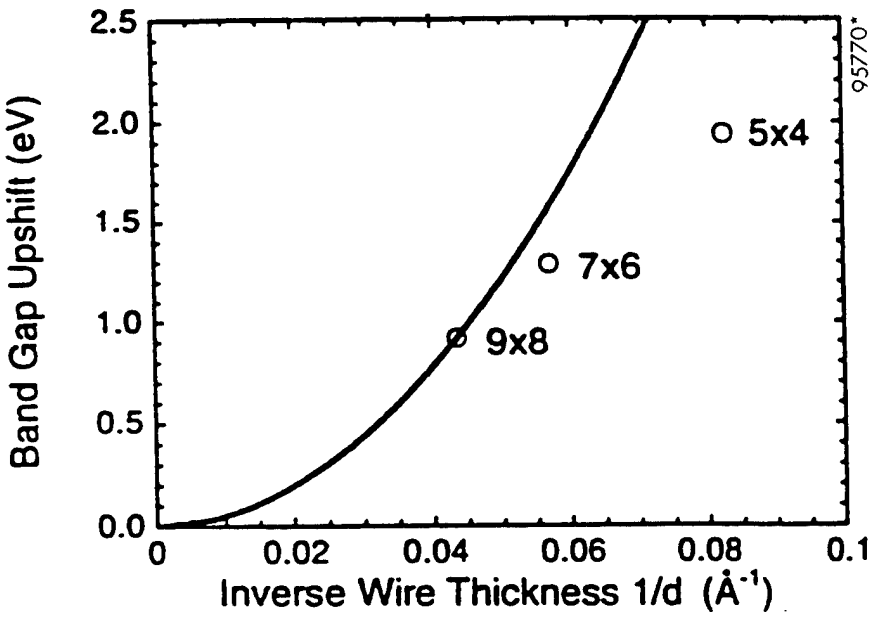
$$E_c = \frac{h^2}{8d^2}\left(\frac{1}{m_{eff}}\right) \qquad (1)$$

where d is the wire thickness and m_{eff} is the effective mass for the band in question. This picture was first applied to porous silicon by Averkiev *et al,*[34] who calculated a wire diameter of 30Å based on the peak of their photoluminescence data (1.67 eV, which is deep red in color).

A first principles calculation of quantum confinement effects in silicon has been given by Read *et al,*[35] and their results are presented in Figure 3a. These calculations were based on a pseudopotential technique, discussed in detail in their paper. Their model is considered a one dimensional wire with an axis in the (001) direction, and (110) planes along the sides. They found that significant values of confinement energies are only found when the wire segment has a diameter less than 100Å, and to shift the band gap sufficiently so as to see visible light emission (*i.e.*, a 1 eV upshift) requires a wire size of 25Å. They also found that, for wire sizes exceeding 25Å, their theory agreed exactly with the simple effective mass theory of Equation (1). However, with smaller diameters, the two approaches differ significantly, and for example, blue light emission at 2.6 eV requires a wire diameter of 15Å.



a)



b)

Figure 3 *Calculated bandgap energies for various silicon crystallites with respect to their diameter (continued on next page).*[35-37]

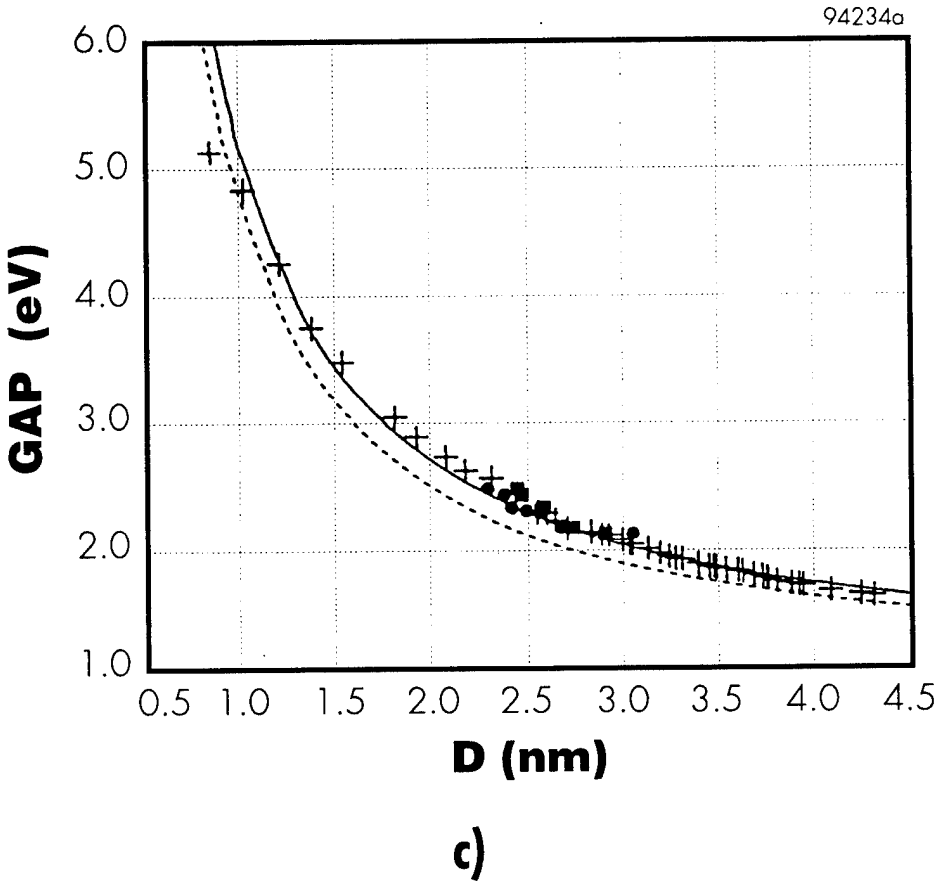


Figure 3 *Calculated bandgap energies for various silicon crystallites with respect to their diameter (concluded).*[35-37]

Another calculation of quantum confinement energies has been given by Sanders and Chang,[36] who used a semi-empirical tight binding model based on silicon atomic orbitals. Once again, they considered a wire progressing in the (001) direction, presenting four (110) faces. Figure 3b shows their results: for a 2 eV band gap, a wire size of about 19Å is necessary. Blue emission at 2.6 eV would need a 13.5Å wire.

As another example, Proot et al used a linear combination of atomic orbitals approach to calculate the confinement energies.[37] Their results are shown in Figure 3c. For emission at 2 eV, this calculation requires crystallites with a 29Å diameter, while 20Å particles should be capable of emitting blue.

These calculations all agree that very small physical sizes are necessary if visible light is to be emitted. The calculations indicate that wire diameters between 12 and 29Å are required for visible light ranging from violet to red. Table 1 indicates how many atomic planes should be present in a silicon wire segment corresponding to the gamut of colors present in visible light. Here, we have taken the average of the three calculations discussed above to relate emission edge to wire size; note that the averages basically agree with the calculations of Read *et al.*[35]

Table 1 *Correspondence between color of emitted light and number of (110) silicon planes in porous silicon.*

Color	Wavelength nm	Energy, eV	Wire diam. Å	No. of Silicon(110) planes
Red	620	2.00	24	14
Yellow	580	2.15	21	12
Green	520	2.40	18.5	11
Blue	480	2.60	16	9
Violet	430	2.90	14	8

If these calculations are correct, then each additional plane of silicon atoms will tune the emission wavelength to the next color.

Suppose a light-emitting device were fabricated as a 1 mm by 1 mm square, and the porous silicon layer was made to be 2.5 μm thick. Since silicon contains 4×10^{22} atoms/cm^3, and if the porosity is 80% (the maximum possible), then the device would contain 2×10^{16} atoms. Next consider that each wire segment that forms the interconnected sponge might be 10 unit cells long, thus containing about 10^3 atoms. This would require 2×10^{13}, or twenty trillion segments. Obviously, no matter how crude the estimate of the number of segments may be, there will be trillions of them, and we need to maintain their thickness to within a single atomic layer if we are to reproducibly choose the color of the emission. This would appear to present a difficult problem.

However, in any unit cell with 108 atoms, 48 of them are on the surface! with 56 dangling bonds present. It is clear that the surface is extremely important, and cannot be ignored.[38] It is probably correct to say that while quantum confinement is necessary in order to separate the conduction band and the valence band edges sufficiently to allow transitions at visible wavelengths, the actual radiative recombination is likely to involve the surface. This may be very propitious, because it seems unlikely that we could effectively control the thickness of the wire structures within individual atomic planes, and thereby tune the color.

2 PHASE II OBJECTIVE

The objective of Phase II work was to develop a basic understanding of the physical phenomena involved in fabrication and operation of ITO/porous Si heterojunction devices, in order to improve their EL efficiencies. In addition, Phase II would also investigate the possibility of true wafer-scale integration of a porous Si-based LED and a Si-based photodetector on a single Si substrate. This study is important because the key to the success of the research on porous Si-based devices lies in the anticipated compatibility of their fabrication processing with bulk Si electronics technology.

3 EXPERIMENTAL PROCEDURE

3.1 Sample Preparation

Anodic Etching - Figure 4 shows the anodic etching system which was used for producing porous Si samples. This system relies on a Keithley Model 225 current source, with the sample connected as the anode (+) and a foil platinum as the cathode (-). The electrolyte, usually a 1:1:2 mixture of hydrofluoric acid (HF), ethanol and H_2O, is contained in a teflon vessel. The silicon wafers were held in a specially prepared jig which only exposes the front surface to the solution, allowing electrical contact from the back, isolated from any liquid. Porous silicon was produced by anodically etching polished p-type Si(100) and Si(111) wafers, with resistivities ranging from 0.1 to 14Ω-cm, at current densities between 2 to 200 mA/cm^2.

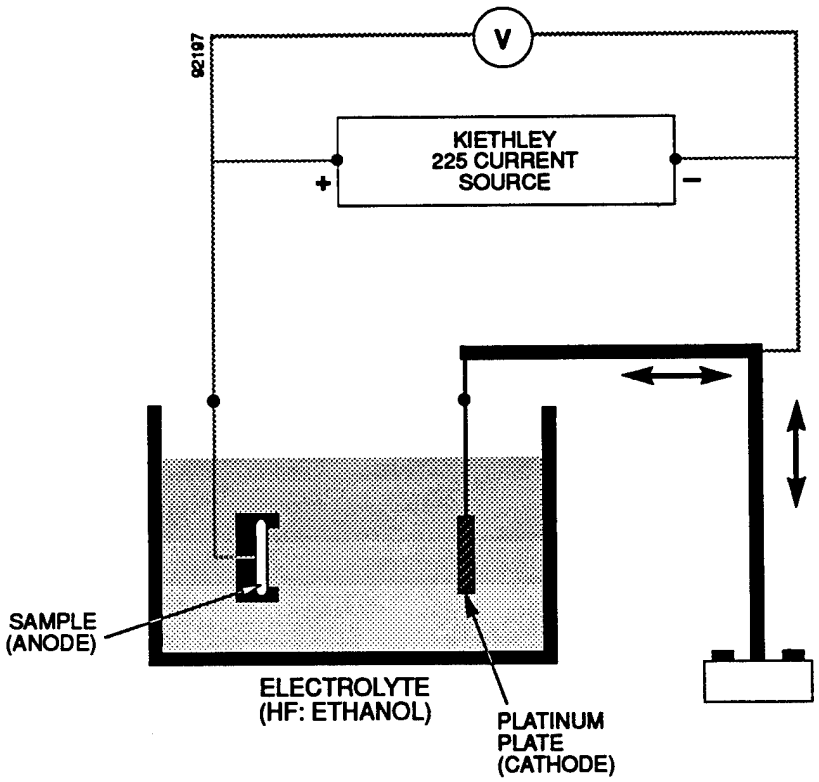


Figure 4 *Schematic diagram of the anodic etching system used at Spire for fabricating porous silicon samples.*

We found that shifts in the emission to shorter wavelengths can be controlled for any sample by increasing the duration of the etch procedure and by allowing the samples to remain passively (with no bias applied) in the HF for periods of time after anodic etching is terminated.

Stain Etching for Fabrication of Visible-light-emitting Porous Polycrystalline Si Layers We have extended our work beyond the study of bulk single-crystal Si substrates and have fabricated luminescent porous materials on thin films of polycrystalline Si deposited onto quartz substrates. The formation of Si-based light-emitting elements on a transparent substrate such as quartz or glass has great potential for the fabrication of low-cost, low-power, high-resolution thin film electroluminescent, cathodoluminescent, or plasma-induced photoluminescent displays.

We demonstrated visible-light emission from porous structures formed in bulk and thin film polycrystalline silicon materials by anodic etching in an $HF:H_2O:C_2H_5OH$, or by stain etching in an $HF:HNO_3:H_2O$ solution. Our results indicated photoluminescence (PL) peaks at wavelengths between 650 and 655 nm, and with intensities comparable to those typically obtained from porous samples of single-crystal silicon. When the porous polycrystalline Si (PPSI) layers formed on a quartz substrate are excited optically, a bright orange-red emission can be viewed through the quartz substrate as well as the front surface. Luminescent PPSI films offer the possibility of monolithically integrating Si-based light-emitters along with recently developed polysilicon thin film transistors (TFT) for a novel, high-resolution, low-power active-matrix thin film electroluminescent (AM-TFEL) flat panel display. Additionally, nanostructures originating from polycrystalline Si substrates may enable low-cost fabrication of highly efficient photovoltaic cells.

Visible Photoluminescence Emission Spectroscopy - PL spectrometry measurements were performed using Spire's PL system, shown in Figure 5. An Omnichrome ultraviolet (325 nm), and an Argon (488 nm) laser were used to excite porous Si. The laser emissions were dispersed with a SPEX Model 1702/04 grating monochromator and detected with a photomultiplier. An EG&G Model 5207 lock-in amplifier interfaced to a Hewlett-Packard Model 86B computer collected the data.

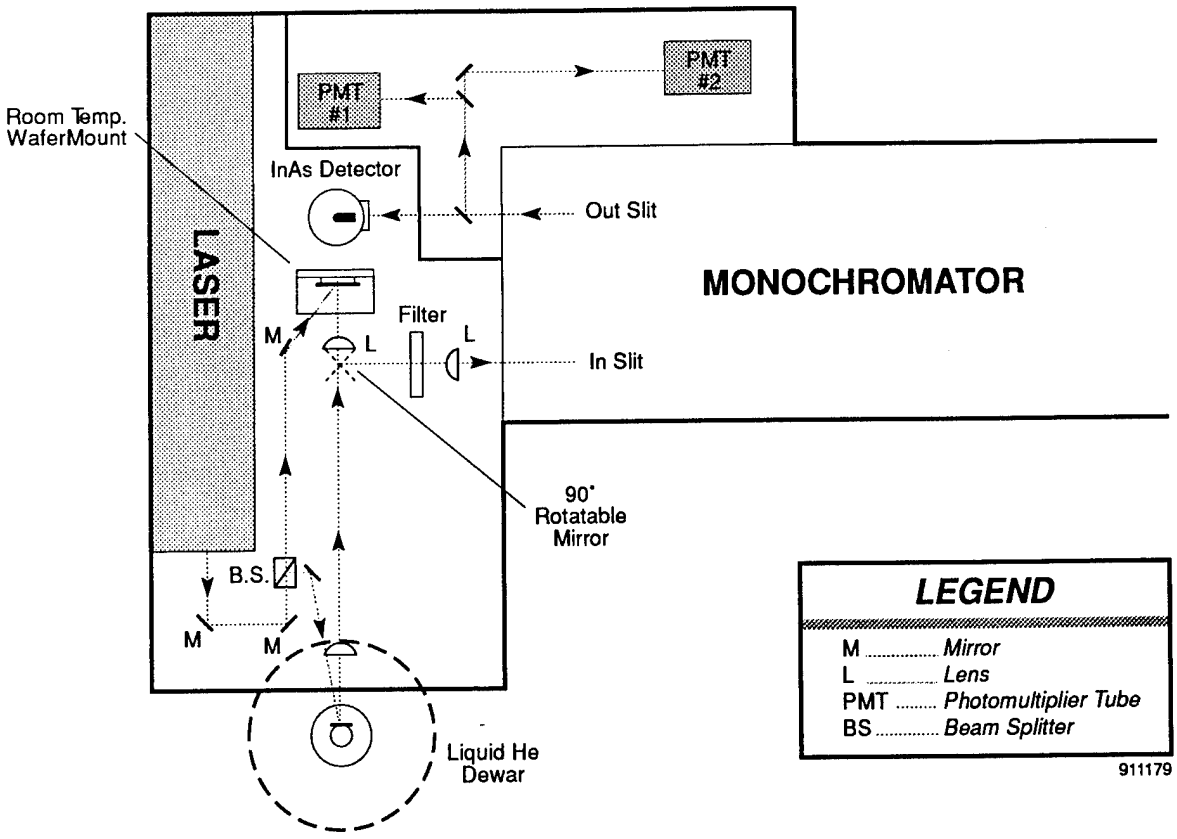


Figure 5 *Schematic of Spire's PL system.*

Infrared Photoluminescence Emission Spectroscopy - Infrared (IR) PL was carried out at Northeastern University in collaboration with Prof. Clive Perry and Dr. Feng Lu. The IR PL was excited with a Coherent Innova 70 Ar^+ laser, and measurements were carried out for laser powers between 30 to 200 mW. An interference band-pass filter was placed in front of the samples to eliminate plasma lines from the laser beam. The samples were illuminated from the porous Si side and IR PL was collected at a near-backscattering geometry. An SPEX 1401 (0.75m) double monochromator equipped with a pair of 600 line/mm gratings was utilized for the IR PL studies. The PL signal was detected by a liquid nitrogen cooled Northcoast Ge detector. A red filter was placed in front of the detector's collecting lens to filter scattering lines from the second- and third-order grating. Both entrance and exit slits of the monochromator were set at 1000 μm, resulting in a spectral resolution of -1 nm.

4 EXPERIMENTAL RESULTS

4.1 Light Emission from Porous Silicon

In this program we have for the first time fabricated yellow- and orange-emitting heterojunction light-emitting diodes (LEDs) based on silicon.[7,8,39,40] These devices, which operated in air at room temperature, were fabricated by depositing a wide bandgap n-type semiconductor (indium-tin-oxide [ITO]) onto the surface of a p-type silicon wafer which had been electrochemically etched to produce a porous layer with nanometer-sized Si crystallites. The use of ITO or other wide bandgap semiconductors[41] (see Table 2) which are transparent to visible light has potential for visible LEDs and display panels. The results from Spire have achieved nationwide media attention through reports in a number of magazines and newspapers including the Wall Street Journal(December 6, 1991, p. B3), Scientific American (March 1992, p. 102), Lasers & Optronics (January 1992 , Vol. No. 1, p. 8), the Electronics Engineering Time (May 25, 1992, p.4), and etc. See attached list of scientific papers published by Spire on this topic, as well as a list of news media.

We studied the porous silicon films before fabricating devices. As shown above, Figure 2 shows photoluminescence spectra of several porous silicon samples formed under different conditions of chemical etching, chosen to provide different wire diameters. (Asymmetries in some curves are an artifact from an optical filter with cutoff characteristic at 520 nm, which was required to stop the direct light from the Coherent Model INNOVA-60 argon ion laser, emitting at 488 nm, from entering the detector.) These red, orange, yellow, and green colors could be clearly identified on samples prepared under different conditions, or spatially separated across the surface of a sample processed with graded properties. Longer etch periods always resulted in blueshifts in the emission wavelengths. The intensity of the photoluminescence was found to be essentially equal in intensity to that of a Spire reference sample of epitaxial $Al_{0.30}Ga_{0.70}$ material. When alloys of silicon/germanium were prepared under identical conditions with pure silicon samples (see Figure 6) the peak wavelength of photoluminescence was always red-shifted, indicating that alloying with Ge tends to decrease the bandgap of these structures. When samples were biased anodically in aqueous NaCl solutions, the surfaces were observed to emit red light (Figure 7), consistent with the report of Halimaoui et al.[6] The properties of this emission were basically similar to the photoluminescence results, and ceased within a few minutes.

Table 2 *List of transparent semiconductors for porous Si-based LEDS, based on Spire's patent.*[41]

P-type Materials			N-type Materials
B-doped	**Mg-doped**	**N-doped**	
C (diamond)	GaN	ZnSe	AlP
	GaP	ZnTe	GaP
	AlP	$CuAlS_2$	ZnS
	SiC	$CuAlS_2$	ZnSe
	Amorphous Si	$CuAlSe_2$	CdS
	Amorphous SiC	$CuGaS_2$	$ZnSiP_2$
		$ZnGeP_2$	$CdSiP_2$
			In_2O_3
			SnO_2
			ITO ($In_2O_3 + SnO_2$)
			ZnO
			CdO
			Cd_2SnO_4
			GaInN
			GaN
			SiC
			Amorphous Si
			Amorphous SiC

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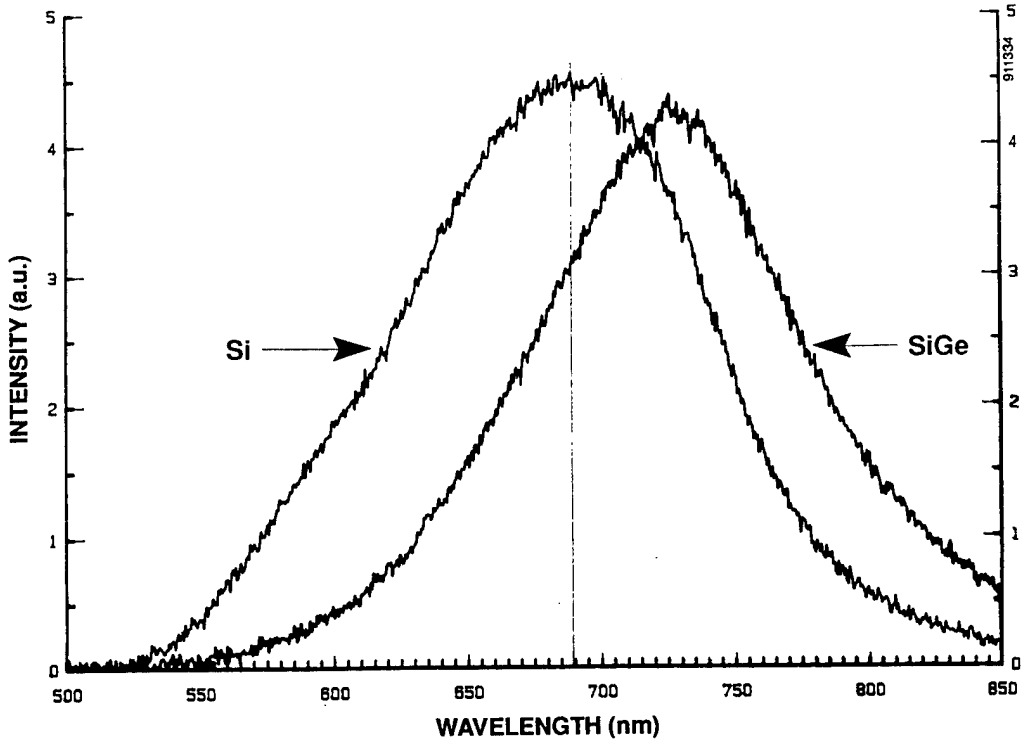


Figure 6 *Comparison of PL from porous Si and a porous structure produced on an epitaxial SiGe film with a 6% Ge concentration.*

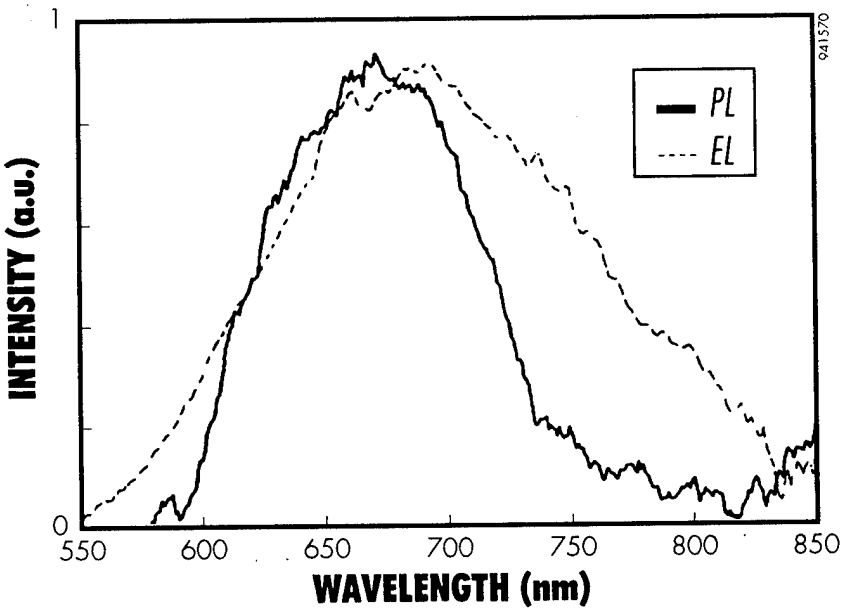


Figure 7 *Comparison of normalized PL and EL spectra from porous polycrystalline Si thin films on ITO-coated glass.*

Solid state ITO/porous-Si devices showed strong rectifying behaviors. Light emission emanating from the top surface through the transparent emitter was only observed under forward bias conditions, and appeared to last indefinitely (at least 84 hours). Photogenerated currents in response to incandescent illumination were seen under reverse biases, although no photocurrents were observed at zero bias, possibly due to a photocurrent suppression mechanism.[42]

Light emission intensities were measured with a Hamamatsu Type R889 photomultiplier; the emission appeared to be centered at about 580 nm. Figure 8 gives a plot of the electroluminescence intensity as a function of diode current for a relatively large porous silicon LED (area =5 mm^2). At currents below about 100mA, the light intensity increases as the square of the current, finally becoming linear in current at higher levels. Such behavior has typically been observed with conventional AlGaAs LEDs, where the low current square law regime is considered to be dominated by recombination at defects in the space charge region, while every injected minority-carrier leads to the emission of a photon at higher current levels.[43]

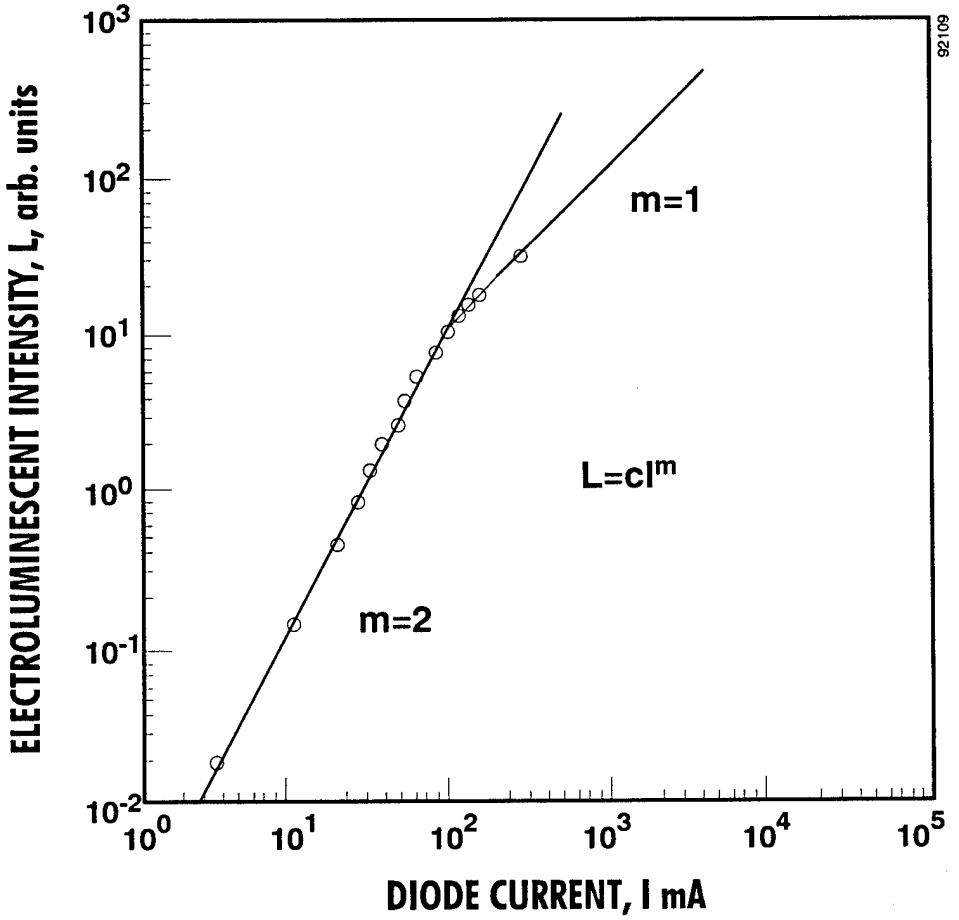


Figure 8 *Dependence of porous Si LED electroluminescence intensity on device current.*

4.1.1 Series Resistance

Our devices displayed excellent rectifying characteristics, and light was only emitted under a forward bias. Only devices based on etched silicon exhibited light emission. A detailed study of room temperature current-voltage (I-V) characteristics for our devices indicates a relatively large value of series resistance R_S for our PS diodes. It is clear that the resistivity is a manifestation of a problem with hole transport through the silicon nanostructures.[44] In fact, Anderson et al.[44] have shown that for lightly doped porous silicon, the resistivity scales directly with the thickness of the etched layer, while the reciprocal of the capacitance is also linearly related to thickness. Therefore, the porous silicon appears to be completely "depleted." We may question what has been "depleted?" In fact, are there any dopants present in the majority of the wire segments, or are they depleted of all dopants? With a doping density of 3×10^{15} boron/cm^3, each dopant occupies 3×10^6 nm^3. Thus if a red-emitting segment has a cross section of 2.5 nm x 2.5 nm, and if on average such segments are 5 nm long (ten unit cells, with each unit 5.4Å long in the (001) direction), each particle occupies about 30 nm^3. So only one in a hundred thousand particles would contain a dopant atom. It is not clear what "depletion" refers to under such circumstances.

Furthermore, according to the above analysis, preferential etching of certain positions at the tip of a pore causes the sponge structure to be generated; it is quite reasonable that the presence of a p-type dopant at the surface will attract a hot hole in transit during the etching process, and therefore, all dopants may be preferentially depleted from the porous structure. If true, then the porous silicon is basically intrinsic material, with a carrier concentration of about 1×10^{10} cm^{-3}. Such a carrier concentration yields a resistivity of about 1×10^6 ohm-cm, consistent with reported data.

Clearly, a fraction of the externally applied voltage will be dropped across the resistance, masking properties at the ITO/porous silicon junction. Therefore, we sought to remove this factor before proceeding to analyze the junction characteristics.

In general, the current-voltage relationship for a junction diode, including the ideality factor m, can be written as,

$$I = I_0 \{ e^{\frac{q}{mkT}(V - IR_S)} - 1 \}. \tag{2}$$

We can explicitly represent the presence of a potential barrier by defining the saturation current as,

$$I_0 = I_{00} \exp[-\phi_b / kT] \tag{3}$$

Then the dynamic resistance of the diode is expressed as,

$$r = \frac{dV}{dI} = \frac{mkT}{qI_0} e^{-\frac{q}{mkT}(V - IR_S)} + R_S = \frac{mkT}{qI} + R_S \tag{4}$$

Clearly, when V (and hence I) becomes large, the first term in Equation (4) will become negligible as compared to the second term, and the I-V characteristic will approach a straight line, with slope R_S. An I-V characteristic for an ITO/porous silicon LED is shown in Figure 9, where curve "a" is the raw data. Relying on Equation (4), we corrected the I-V characteristic to obtain the dependence of the current on the junction voltage. An exponential regression analysis of the corrected data yielded curve "b" in the figure, which indicates the flat band potential of the junction is achieved at about 3 volts forward bias. Thus the device should begin to emit light with about 3 volts applied to the junction, and if R_S can be significantly reduced, with less than 5 volts total bias. Large applied biases that are shown in Figure 9 are simply dropped across the series resistance, not across the junction.

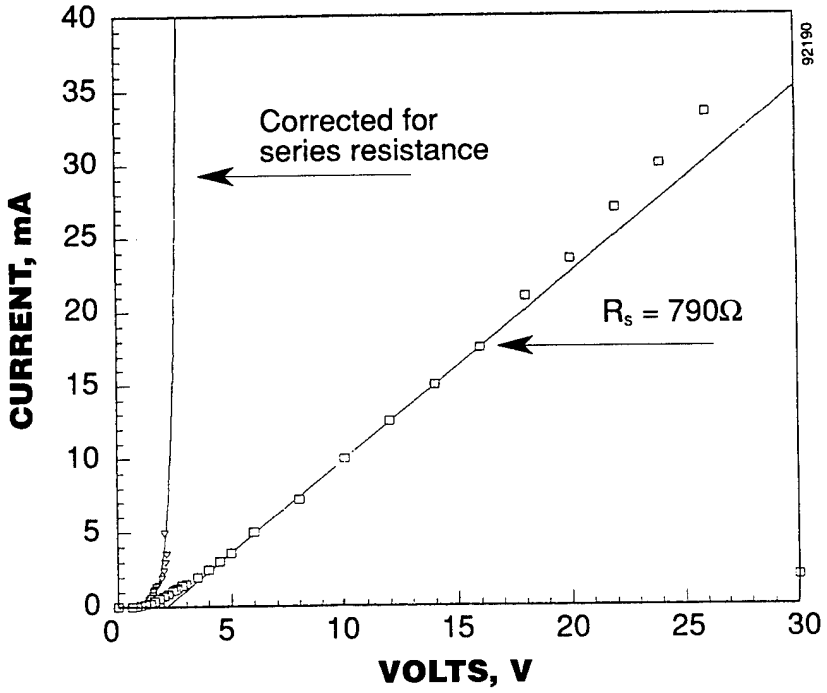


Figure 9 *Current-voltage characteristics of porous-silicon LED, indicating presence of series resistance, corrected plot implies that junction voltage for light emission can be less than 3V.*

4.1.2 Surface States

We fitted our corrected data to Equation (2), with the R_S term now eliminated. The results of our analysis are displayed in Figure 10. At biases greater than about 0.5 V, the data indicates an ideality factor m of 8.4 over three decades of current. At lower applied voltages, the data can be fitted with a significantly smaller ideality factor m = 3.8. Ideality factors greater than 2 but less than 4 are often found with junction diodes formed between standard crystalline silicon and transparent conducting oxides such as ITO or SnO_2,[45] and their dependence on interfacial charges has been explained by Maruska and coworkers.[46]

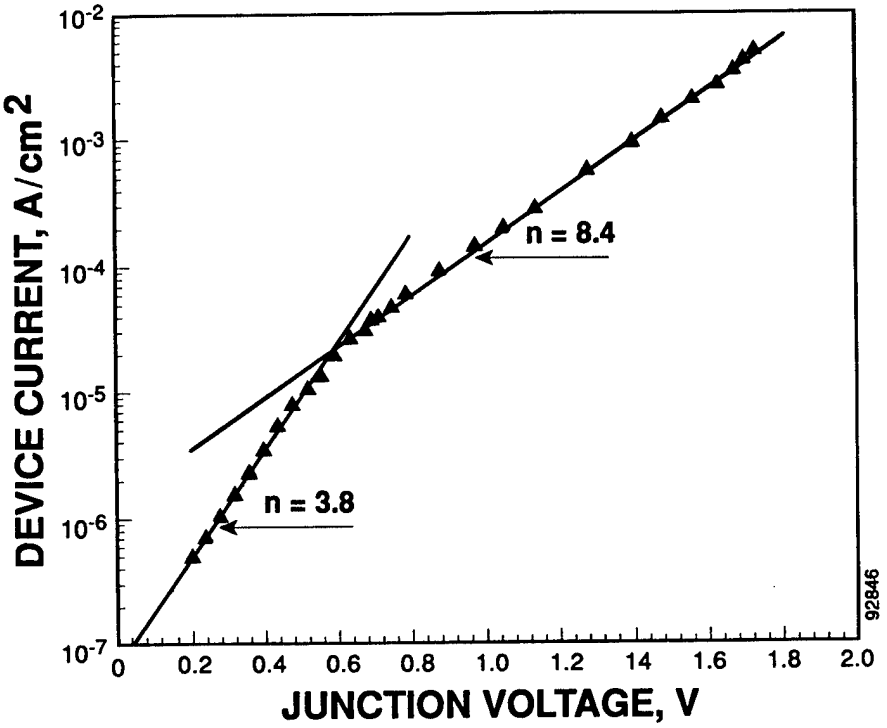


Figure 10 *Current-voltage characteristics of a porous silicon LED, showing diode ideality factors dependent on densities of interface states.*

Based on the theory of Card and Rhoderick,[47] we can explain the origin of the diode ideality factor for conducting-oxide/porous silicon diodes as follows. We note that in general, after the porous silicon sample is removed from the electrochemical processing environment, it is typically exposed to the ambient atmosphere. Therefore, almost certainly a thin film of native silicon oxide will form over the entire surface. If there are interface states that have formed between the silicon and the silicon oxide, then as long as the oxide is thin enough to allow equilibrium between the ITO and the porous silicon to be achieved, matching of the fermi levels will require that negative charges be transferred from the ITO conduction band both to the interface states and to the valence band of the porous silicon. Therefore a potential of magnitude V_S will be present across the native oxide. Application of a forward bias will serve to decrease the magnitude of stored negative charge in the interface states, and thus change the magnitude of V_S. Essentially, the diode ideality factor indicates the proportion of the applied voltage which will fall across the oxide layer.

The model we use considers three regions existing in series which constitute the device, and an applied external bias is divided among these three regions, so that,

$$V = V_R + V_S + V_D \tag{5}$$

The first region represents the linear series resistance R_s, found in the bulk of the porous silicon. By accounting for any series resistance, this fraction of the voltage, V_R, may be eliminated from further consideration, as we have done above. The second portion of the applied voltage falls across the space charge region in the semiconductor, and therefore serves to change the diffusion

potential, V_D, and if these surface states can be charged, then the third potential drop, V_S will be present across the thin oxide film. We take the presence of interface states, which have a density D_{ss} ($cm^{-2}eV^{-1}$), to be necessary to explain our experimental results. The interface states are available to store charge at the semiconductor boundary; w is the width of the semiconductor space charge region, and ε_i, ε_s are the dielectric constants for the insulating oxide and semiconductor regions, respectively. However, we stress that the presence of the interface states has deleterious consequences for device performance.

Therefore, applying these results to porous silicon LEDs, the ideality factor m can be expressed as

$$\begin{aligned} \Delta V_D &= \frac{\Delta V}{m} \\ \frac{1}{m} &= 1 + \frac{dV_S}{dV} \end{aligned} \tag{6}$$

From Gauss' Law applied across the porous silicon interface,

$$\begin{aligned} V_S &= (\frac{\delta}{\varepsilon_i})Q_I \\ &= (\frac{\delta}{\varepsilon_i})(Q_{ss} + Q_d) \end{aligned} \tag{7}$$

where Q_I is the charge in the degenerately n-type ITO, Q_{ss} is the charge stored in the interphase layer and Q_d is the space charge in the semiconductor. Clearly,

$$Q_I + Q_{ss} + Q_d = 0. \tag{8}$$

Therefore, when a voltage V is applied, the change in V_S is given by,

$$\begin{aligned} \frac{dV_S}{dV} &= \frac{\delta}{\varepsilon_i}[\frac{dQ_{ss}}{dV} + \frac{dQ_d}{dV}] \\ &= \frac{\delta}{\varepsilon_i}[\frac{dQ_{ss}}{dV_D}\frac{dV_D}{dV} + \frac{dQ_d}{dV_D}\frac{dV_D}{dV}] \end{aligned} \tag{9}$$

which assumes that V_D is a function of both Q_{ss} and Q_d. Since

$$\begin{aligned} \frac{dQ_d}{dV_D} &= \frac{\varepsilon_s}{w} \\ \frac{dQ_{ss}}{dV_D} &= qD_{ss} \end{aligned} \tag{10}$$

finally it is found that

$$m = 1 + \frac{\delta \epsilon_s}{w \epsilon_i} + \frac{\delta q D_{ss}}{\epsilon_i} \qquad (11)$$

Clearly, large concentrations of charged defects will lead to large values of m.

If m = 3.8, ϵ_i = 3.9, ϵ_s = 11.9 and δ = 2.5 nm, then from the low voltage region of the I-V curve, D = 2.4 x 10^{13} /cm^2eV; we note that Feng et al[48] have reported a value of m = 3.44 for an MIS diode consisting of SnO_2 deposited on c-Si, where such high values of n were attributed to high densities of interface states.[49] At higher applied biases, the even larger values indicate that truly large densities of surface states are encountered. As the fermi level attempts to approach the valence band with increasing forward bias, it effectively becomes pinned by the surface states.

We note that we also considered that the current transport might be controlled by tunnelling at the heterojunction, whereupon we would expect the current-voltage characteristics to follow the Fowler-Nordheim Equation, *viz,*[50]

$$I = AV^2 \exp(-\frac{V_0}{V}) \qquad (12)$$

An attempt to fit the data to this format was unsuccessful, indicating that tunnelling is not the controlling mechanism.

4.1.3 Thermal Activation

If current in a diode is controlled by carrier injection over a potential barrier, then we expect the process to be thermally activated. Therefore, we measured the current-voltage (I-V) characteristics of our diodes over a range of temperatures, from 190 to 325K. Samples were placed onto a temperature-controlled large copper mass which was positioned in an evacuated chamber. The actual device temperature was monitored with a thermocouple placed in contact with it in the measurement chamber.

The current-voltage characteristics of a representative ITO/porous silicon LED are shown in Figure 11. Current rather than current density is reported because the surface area of the etched silicon which actually contacts the ITO is interterminate.[51] An exponential regression program was used for analyzing the data. It was determined that at any temperature, the data could be fit to a function of the form of Equation (2).

At all temperatures we find that the data can be represented by taking the diode ideality factor as m = 3.0. The regression program was then used for determining the saturation current, I_s, at each temperature. These values are presented as a function of reciprocal temperature in Figure 12, where a good straight line fit to the data is evidenced. These results indicate that the current transport mechanism indeed involves a thermally activated process, with an activation energy of 0.42 eV. This is the barrier to hole flow in the valence band; at these low applied voltages, electrons are not being injected into the conduction band, and we have not observed measurable electroluminescence at such low biases. Note again that an activation energy of 0.42 eV would not be consistent with a tunnelling mechanism of current control.

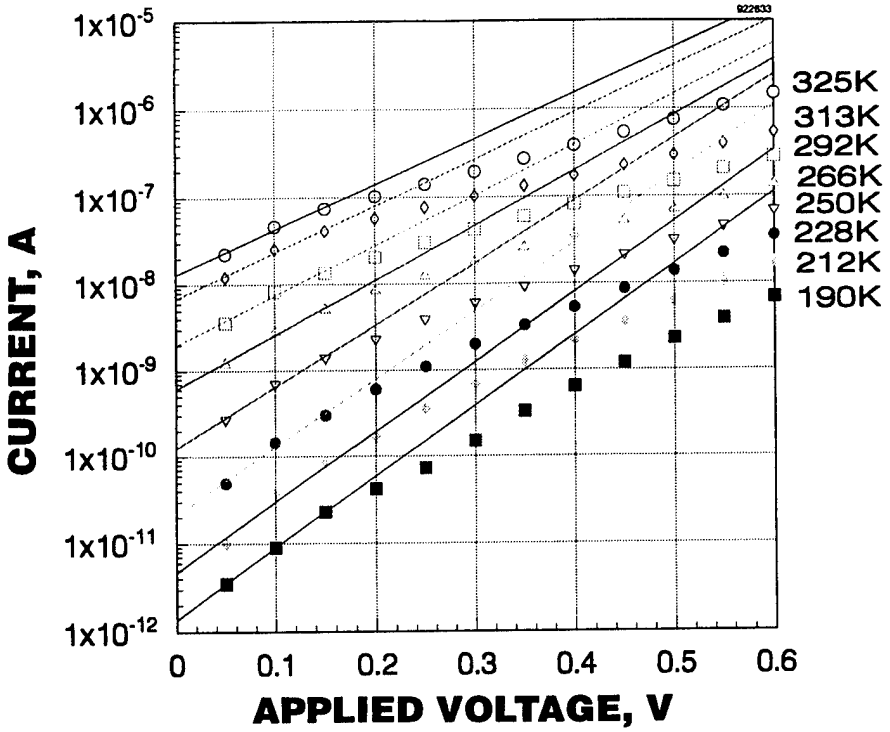


Figure 11 *I-V data of PS LED between 190K and 325K.*

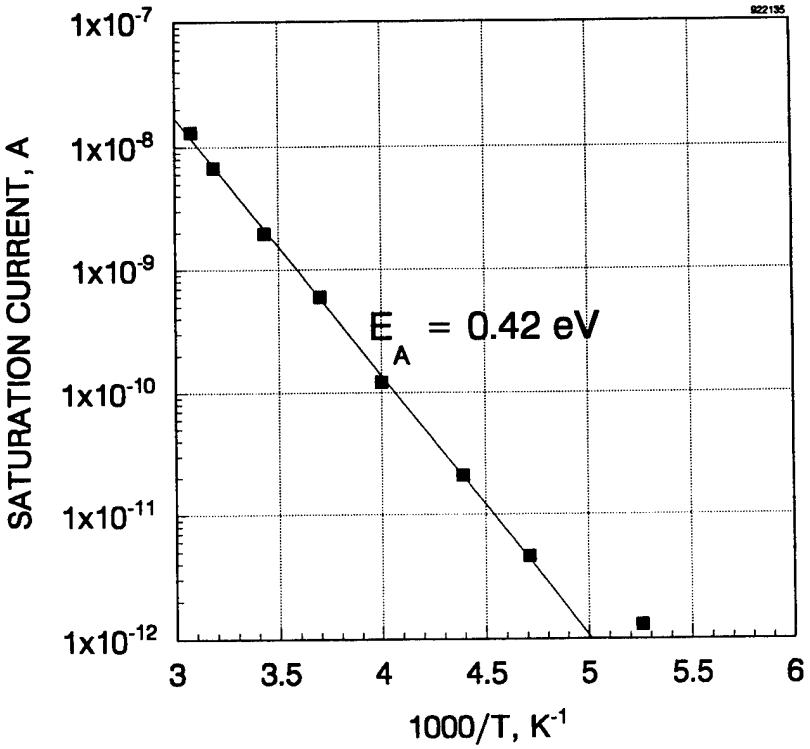


Figure 12 *Temperature dependence of the diode saturation current for ITO/QC-silicon heterojunctions, indicating a barrier height of 0.4 eV.*

Similar measurements and data analysis were also performed on the ITO/bulk-Si devices that were also produced on the same wafer. The current-voltage characteristics were basically similar and the data could be fit using a diode ideality factor on the order of 3; however, for these bulk silicon diodes, we obtained an activation energy of 0.25 eV (shown in Figure 13).

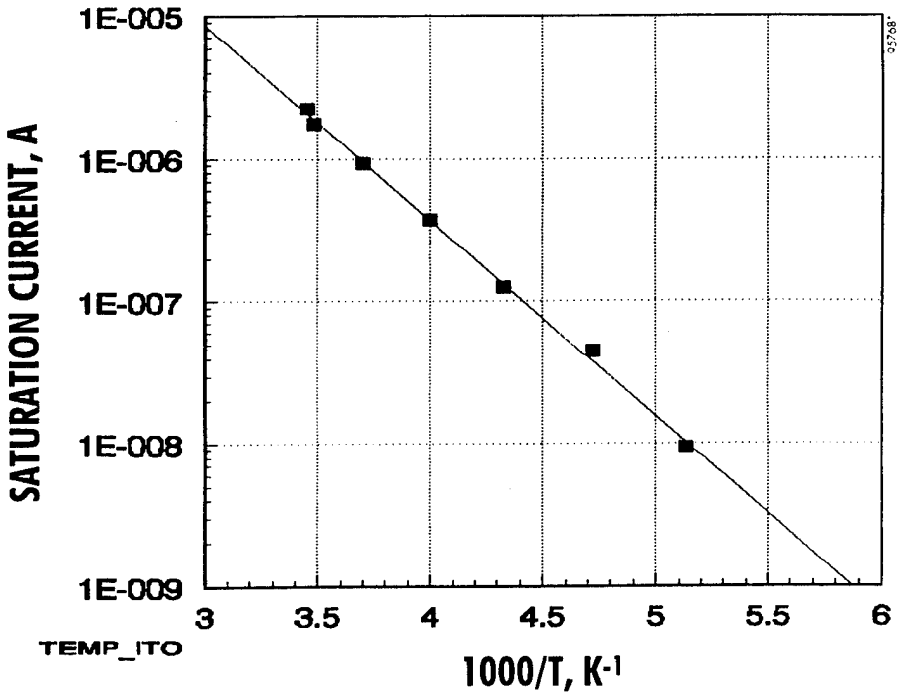


Figure 13 *Temperature dependence of the diode saturation current for ITO/bulk-silicon heterojunctions, indicating a barrier height of 0.25 eV.*

4.1.4 Model for Injection Luminescence in Porous Silicon

In light of these observations, we wish to propose the following model for the operation of our porous silicon LEDs, based on the band diagrams shown in Figure 14. We consider the porous silicon wires will have an initial graded thickness dimension at the interface with the bulk material (refer to any of the earlier structural figures), so that there are no spikes in the band energy diagram. As the wire diameter quickly widens, it grades into the same band gap as bulk crystalline Si. In the sponge area, we expect to find a significant increase in the band separation, due to the quantum confinement effect. This leads to a slope in the potential in both the valence band and the conduction band, with the gradients for both electrons and holes being in the same direction. The energy bands before contact is established between the ITO and the silicon, are shown in Figure 14a. Values for the physical constants of the materials follow the work of Shewchun et al.[52] Based on these values, if there were no surface states to contend with, then the potential barrier in the valence band would be about 1 eV. Thus an np homojunction would be induced in the porous silicon; such an induced np homojunction has been observed in a junction between ITO and bulk crystalline silicon.[52] This hypothetical case for porous silicon is shown in Figure 14b: there could be no hole extraction, only electron minority-carrier injection, with high electroluminescence efficiency.

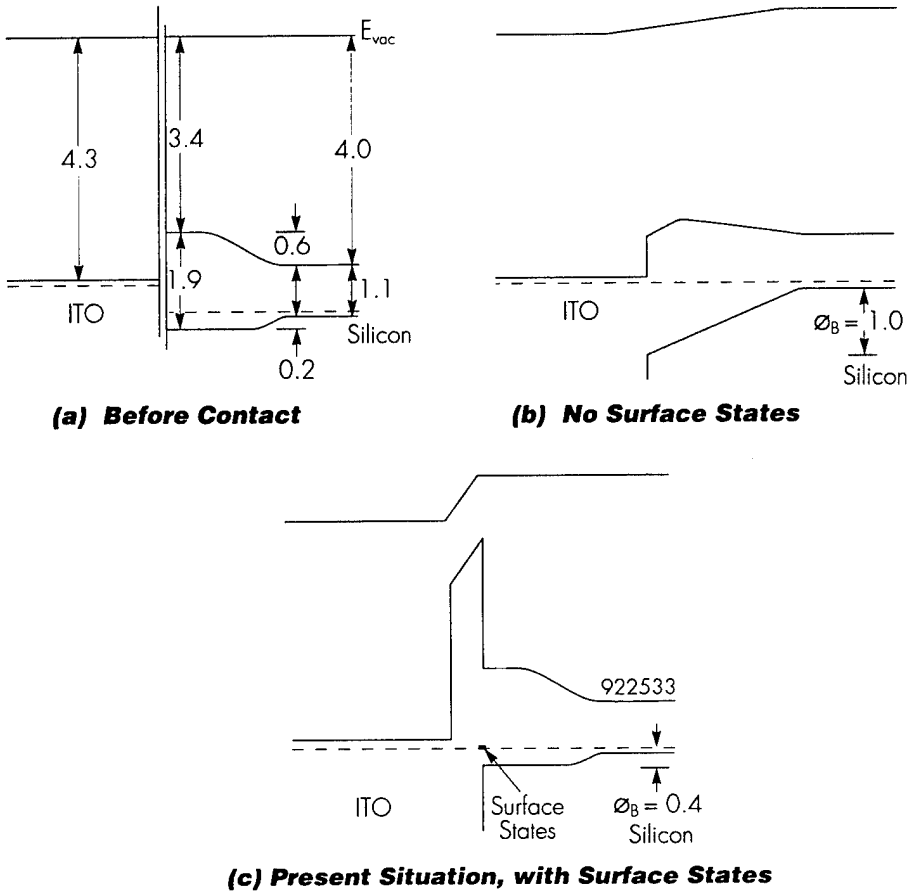


Figure 14 *Energy band diagrams for ITO/PS heterojunctions.*

At present, the high density of surface states leads to the potential energy diagram of Figure 14c. The valence band barrier is only 0.4 eV, and holes are more easily injected into the intrinsic porous silicon material under forward bias than electrons. Therefore, holes must drift under the action of the applied field through the entire "depleted" material. Finally, they are able to recombine non-radiatively with electrons from the ITO through the surface states. This process not only gives a poor radiative recombination efficiency, but is the origin of the series resistance. In a simple bulk silicon PIN diode, the I-region does not constitute a series resistance: our calculations show that so long as equal numbers of holes and electrons are injected by the contacts into the intrinsic material, no matter how wide it may be, the region is electrically neutral, with no electric field present, and the current-voltage characteristics show no problem with a series resistance from the I-layer. As soon as we impede the injection of one carrier type in our calculations, a field appears in order to drive the other carrier, and the resistance of the I-layer must be taken into account.

Therefore, the properties of the contacts to porous silicon are critical to device performance. If equal densities of holes and electrons can be injected into the porous layer, the series resistance problem will be abated. Clearly, the effect of surface state recombination must be eliminated before equal densities of both carrier types can be made available.

4.2 Material Characterization of a working porous Si LED

High resolution cross-sectional electron microscopy (XTEM) and electron diffraction of an np heterojunction porous Si device, capable of emitting light at visible wavelengths, clearly indicates the presence of Si nanostructures within the quantum size regime. These results indicate that the quantum confinement effect is at least partially responsible for photoluminescence at visible wavelengths.

Experimental Demonstration of Quantum Confined Particles - The structure of porous silicon has been studied by XTEM.[4,17,20,53-59] However, here we report XTEM results for a working porous Si device. XTEM results from a visible light-emitting porous Si device were not only essential to relate electrical and material properties, but also provided a unique opportunity to verify accurately the existence of silicon nanostructures, required for quantum confinement at the porous Si/ITO interface. This was possible because the ITO layer protected silicon nanostructures from oxidation and physical damage during and after TEM sample preparation, thus enabling us to observe the tip of the pores at the interface with ITO.

XTEM samples were prepared using standard methods. Two pieces of the sample were glued face-to-face. Slices were cut from this block, metallurgically polished, dimpled on one side using a ball grinder, and thinned to electron transparency using ion milling.

Figure 15 shows a typical porous Si layer with a thickness of about 6.5 μm. The porous layer is fairly uniform, though its thickness varies slightly from point-to-point.

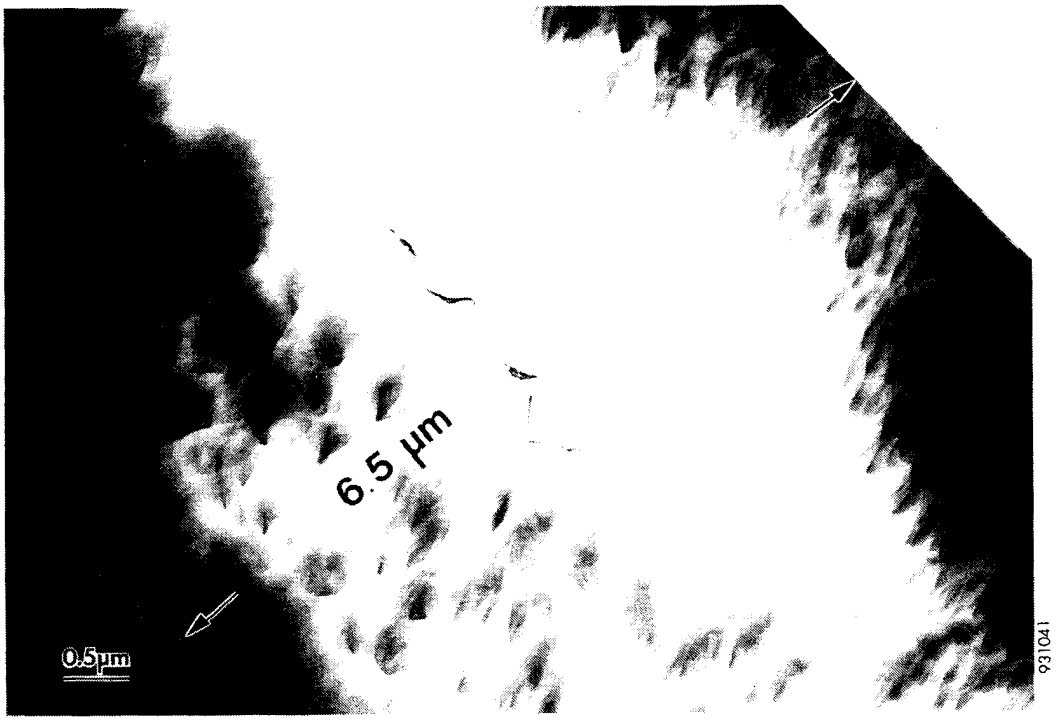


Figure 15 *XTEM of a typical porous Si layer without ITO.*

Figure 16 shows an XTEM of the actual working device. The dark layer on top is the ITO which does not thin as readily as the silicon underneath it. The ITO layer has remained electron-opaque in this particular area of the sample. In other areas of the sample where the ITO is electron-transparent, we are able to distinguish its internal microstructure. Below the ITO layer is the porous silicon layer which consists of two regions. Adjacent to the ITO layer is ~1000Å thick region composed of primarily vertical pores perpendicular to the original sample surface. Below this region is the remaining porous Si. This region consists of an amorphous material with small Si nanocrystals embedded throughout its volume.

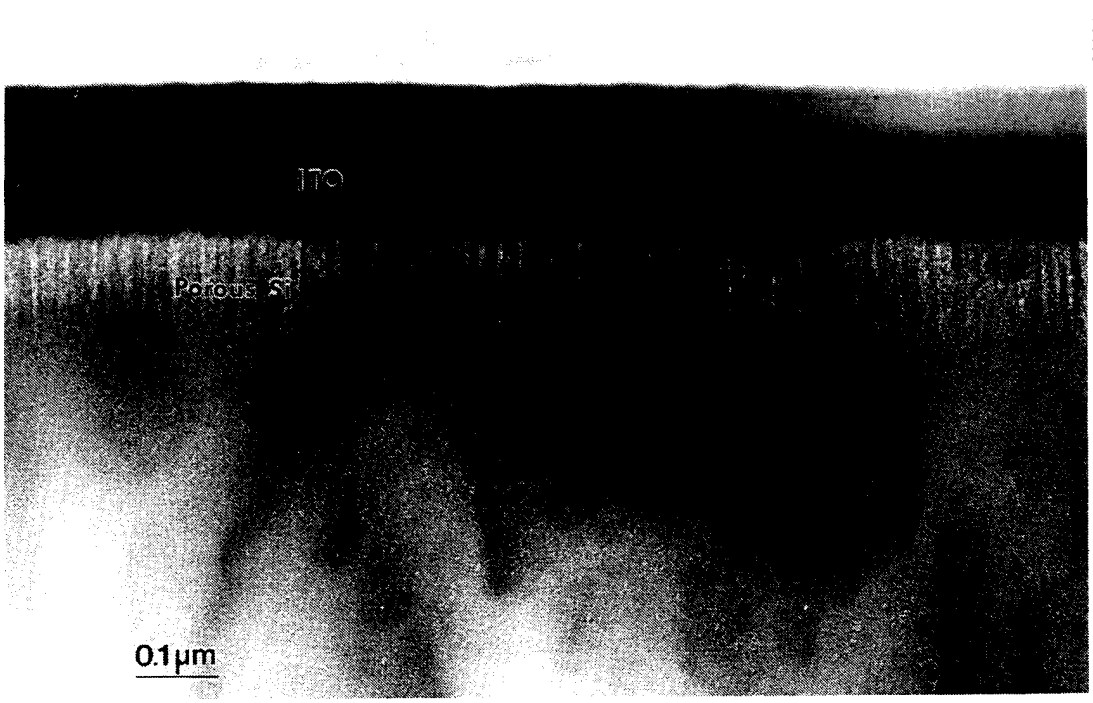


Figure 16 *Cross-sectional view of a porous Si LED determined by TEM.*

Figure 17 shows a high magnification lattice image of the porous silicon layer. The background microstructure is primarily amorphous; however, embedded within this amorphous material are a number of very obvious "dark spots." These dark spots are small single silicon crystal particles with average diameters of about 20 to 50Å. Their diameters are within the quantum confinement size regime. Note that all of the particles are still aligned with the silicon substrate.

Figure 18 is a room temperature PL spectrum for the ITO/porous Si device whose XTEM microstructure is shown in Figures 15 and 16. The spectrum shows fine structures superimposed on a larger main peak. We have found[60] that the spacing between the smaller maxima (fine structures) is reproducible and independent of the main peak energy and sample history. In addition, the energy steps between the smaller maxima correlate with differences in the exciton energies due to the change in the sizes of the quantum wires by complete monolayers of atoms. Optical interference[61,62] at thin surface-layers cannot be responsible for the small variable peaks, as optical interference would produce equidistant peaks due to the constant layer thickness of a sample. Furthermore, the peak-distance should change from sample to sample because of different layer thicknesses; however, neither this nor optical interference were observed.[20]

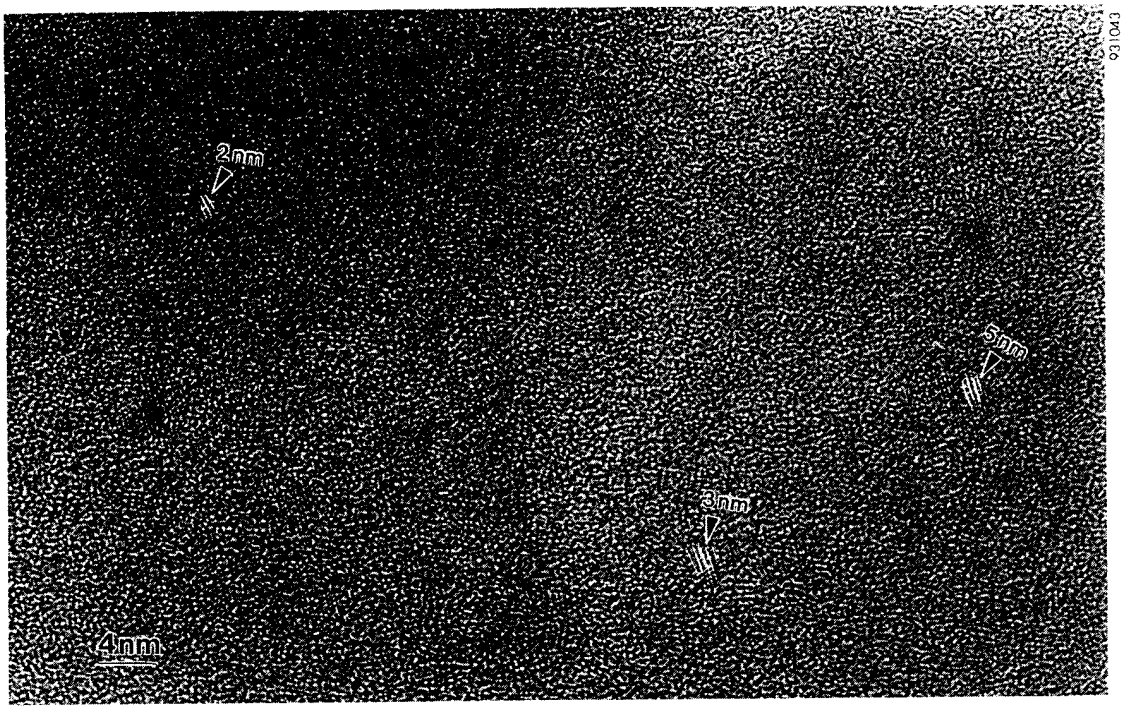


Figure 17 *XTEM micrograph showing the lattice image of a porous Si layer.*

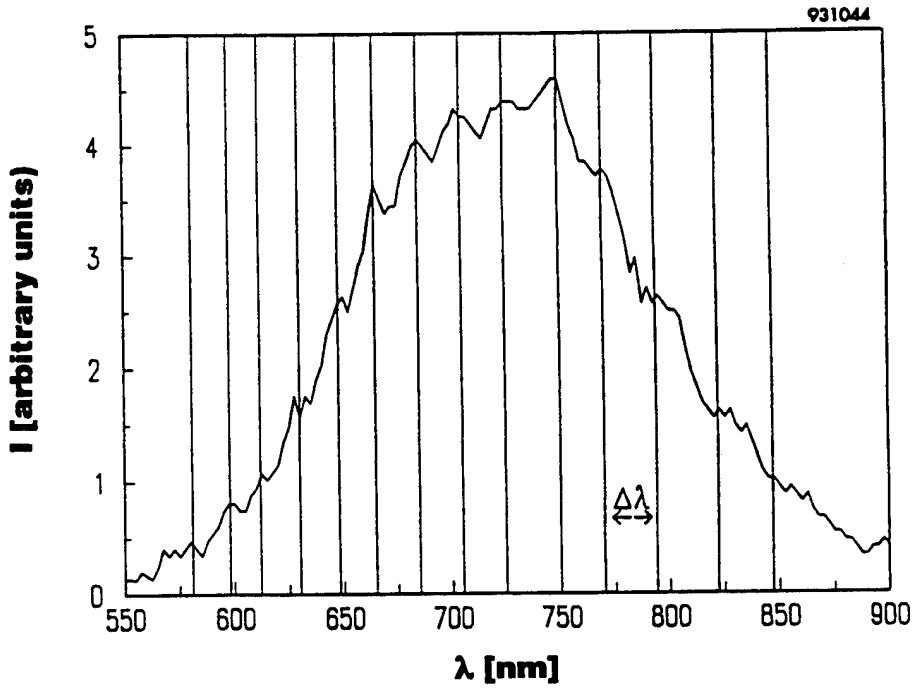


Figure 18 *Room temperature PL spectrum for a working porous Si device.*

Figure 19 is an electron diffraction pattern of the porous silicon region and shows what is expected from Si with bulk properties. The spots observed in the electron diffraction pattern clearly indicates the presence of single crystals in the porous region. The orientation shown in this micrograph is [110], as we are observing a cross section of [100] material. However, [200] spots, normally seen in thick materials, are not observed. The [200] spots are caused by double diffraction, which requires multiple scattering of electrons. The 20 to 50Å diameter Si nanocrystals in the porous-Si layer are too small for double diffraction to occur.

Similar effects have been observed for Si nanocrystals fabricated using other procedures. The lack of [200] spots further supports our idea that the particles are very small and that the diffraction observed was only from the particles and not due to a residual Si substrate.

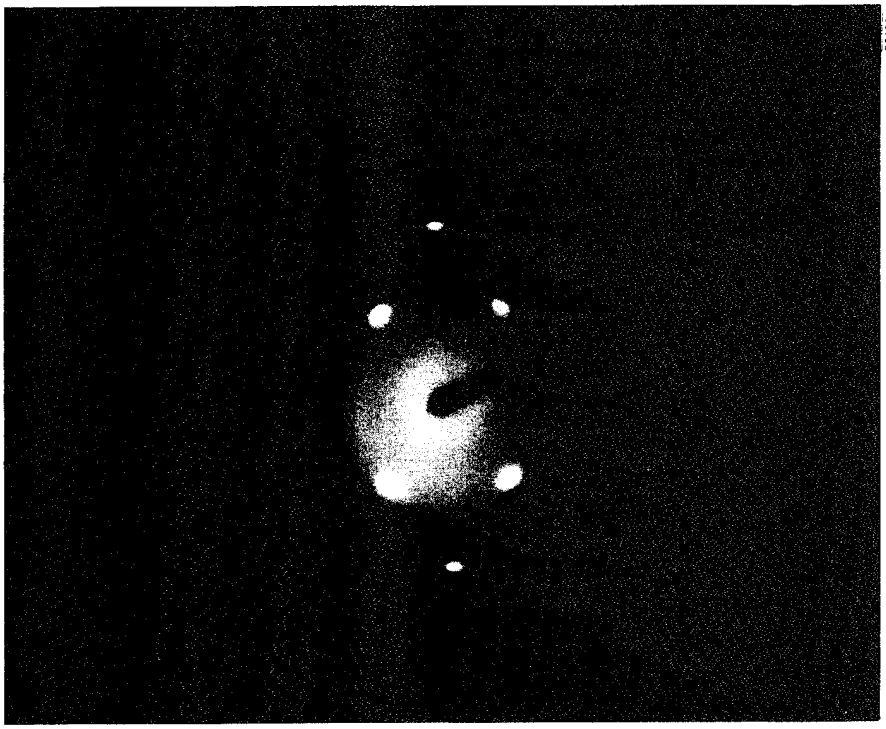
Examination of the single crystal silicon particles in Figure 19 shows the spots slightly spread out into arcs. There are two explanations for this observation:

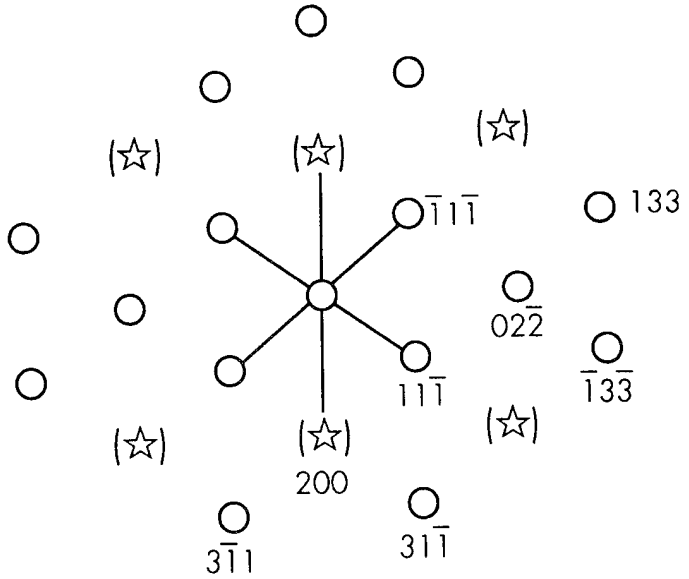
Small Particle Size - The size of the diffraction spots in reciprocal space is inversely related to the particle size, *i.e.*, the smaller the particles causing the diffraction, the larger the spots observed in the diffraction pattern.

Shifting Particle Orientation - Slight misorientation of the Si nanoparticles may be caused by the volumetric expansion caused by oxidation of the silicon so that they are no longer exactly oriented along [110]. This would also result in larger diffraction spots as observed.

Figure 20 shows a high magnification view of the interface between the ITO and the porous silicon. As expected, the surface of porous silicon is very rough. The ITO layer covers all the hills and valleys of the surface and replicates it quite well. In addition, there is no evidence of voids or any other layer between the ITO and the porous silicon. Lattice images of the ITO were obtained; however, we were unable to obtain lattice images of the nanoparticles (silicon) in this area. Assuming the dark particles in the figure are actually single crystal silicon nanoparticles, a direct contact appears to have been made between the conducting ITO and quantum-confined particles. This is consistent with our recently developed tunneling model[7,39] based on our electrical measurements.

In summary XTEM micrographs of an np heterojunction porous Si/ITO light-emitting device indicated that the porous silicon layer consists of two layers. The top 1000Å contains vertical pores perpendicular to the sample surface. The rest of the porous Si layer consists of an amorphous matrix plus embedded Si nanocrystals. High magnification lattice imaging of the porous silicon layer clearly indicated the presence of single crystal particles with dimensions of 20 to 50Å which were aligned with the original silicon substrate orientation. This microstructure is consistent with detailed analyses of electron diffraction patterns of the porous region as well as fine structures observed in room temperature PL spectra. These results clearly indicate that the quantum confinement effect is at least partially responsible for visible luminescence of porous silicon.





☆ Spots that could arise from double diffraction obtained from *Practical Electron Microscopy in Materials Science* by J.W. Edington

Figure 19 *Electron diffraction pattern of the porous Si layer and crystalline Si.*

Figure 20 *XTEM micrograph showing the interface of the ITO and porous Si.*

4.3 Green Blue Emission from Porous Silicon

One of the major factors presently preventing the realization of stable blue-green light-emitting devices using porous Si material is the required limitation of the physical size of the Si nanostructures necessary to expand the bandgap into the blue wavelength range. The blue-green emitting crystallites formed in porous Si are presently too fragile and unacceptably susceptible to environmental effects during the processing steps required to fabricate EL devices. Spire believed, however, that this problem could be solved either by:

a) increasing the base bandgap of the bulk material using chemical vapor deposition of Si-C random alloy layers prior to forming quantum-sized structures. The initial increase in the bandgap of the pre-etched wafer would permit larger "quantum wires" or nanostructures to yield the energy gap required for blue- or green-emitting crystallites; or

b) creating a SiC phase by carbon implantation and annealing, after the formation of red-emitting Si nanostructures.

This work included the growth of Si-C random alloy layers, with thicknesses of 10 μm, using chemical vapor deposition in order to enlarge the bandgap of the base material prior to anodic etching, and also carbon implantation into red-emitting Si nanostructures to obtain blue-green emission. These approaches are summarized in Figure 21.

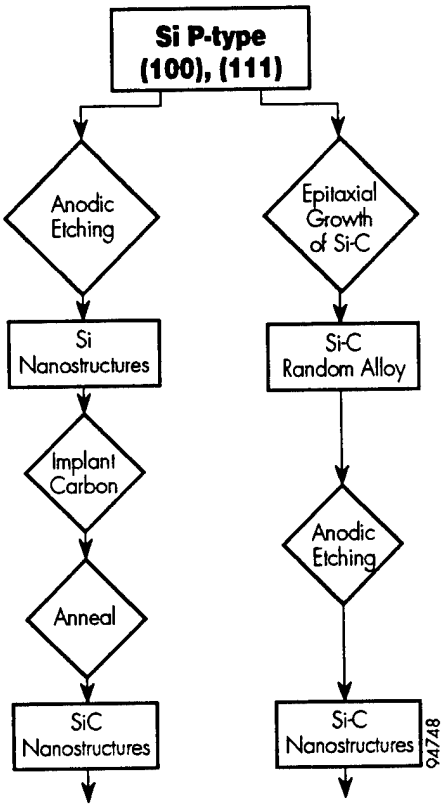


Figure 21 *Flowchart of approaches used to achieve blue-green emission from porous Si.*

4.3.1 CVD Growth of Epitaxial $Si_{1-x}C_x$ Layers

We have grown epitaxial Si-C alloy layers using an in-house AMC 7600 CVD reactor with methane (CH_4) and trichlorosilane ($HSiCl_3$) as gas sources. Epitaxial SiC layers about 10 μm thick were grown on p-type <111> Si wafers using various methane flow rates. The materials were grown in a temperature range of 1053°C to 1120°C. Several material and electrical characteristics were performed immediately after the growth process.

4.3.2 Carbon Implantation and Annealing

Implantations were accomplished on Spire's high current ion implanter. The beam is generated by an Eaton NV 10-160 joined to a Spire-designed endstation.

Following the formation of porous Si layers we implanted carbon into porous layers and bulk Si substrates. Silicon was implanted with doses ranging from 1×10^{16} to $1.5 \times 10^{17} C^+/cm^2$ at energies from 50 keV to 200 keV. After implantation samples were annealed in an in-house tube furnace to form SiC. Samples were annealed in a nitrogen ambient at temperatures ranging from 620°C to 1300°C for approximately 30 minutes to 3 hours.

In the following we report photoexcitation results for visible and infrared emission from carbon-implanted red-emitting porous Si and anodically etched SiC random alloys which were grown epitaxially by CVD.

4.3.3 Characterization Si-C Random Alloy Porous Structures

Posthill *et al.*,[63] have reported the growth of C_xSi_{1-x} epitaxial films on Si<100> by remote plasma-enhanced CVD. Carbon concentrations of (approximately) 3 atomic percent were achieved at a growth temperature of 725°C. At IBM[64] pseudomorphic (strained layer super-lattices) $Si_{1-x}C_x$, with $x > 0.02$, has been grown on Si <100> using Solid Source Molecular Beam Epitaxy.

We have grown epitaxially Si-C random alloy layers, with thicknesses of 10 μm, on two- and four-inch Si wafers using chemical vapor deposition (CVD). Lattice contraction caused by carbon doping of Si <111> has been determined by rocking curve measurements using Cu $k_{\alpha 1}$ radiation and (333) reflections. The perpendicular lattice constant mismatch between the substrate and the Si-C layer varies linearly with the carbon doping level. Assuming that interstitial carbon has no effect on the lattice constant, the relationship between the mismatch $\Delta a/a_0$ (ppm) and carbon doping N_c (cm^{-3}) is given by:[65]

$$N_c = -4.13 \times 10^{16} \frac{\Delta a}{a_0} \qquad (13)$$

$\Delta a/a$ = -260 ppm, which indicates that the carbon concentration (N_c) is about 1.07×10^{19} cm^{-3}, which corresponds to 0.02%.

The Si-C samples were etched using our standard anodic etching conditions and, we have observed very strong red photoluminescence. Figure 22a shows a PL spectrum of one of these samples (sample F2019B), which was excited with a 9 mW UV laser at 325 nm. Generally, we excite our porous Si samples with an argon laser at 488 nm, but we used a UV laser in anticipation of a possible blue shift in the spectra. From the porous Si spectrum in Figure 22a we cannot conclude whether a blue or red shift occurred due to the growth of epitaxial Si-C.

Because the intensity of PL emission is dependent on doping level and etching conditions, a direct comparison of intensity and peak position of these samples, with those from standard silicon samples, is impossible. Only a qualitative comparison can be made. During the past few years, we have etched several hundred Si wafers with different doping levels and under different conditions. This red PL appears stronger to us than any previously observed samples prepared under any etching conditions.

Comparison of the PL from porous epitaxial Si-C with that from a standard $Al_{.30}Ga_{.70}As$ sample (see Figure 22a) shows that the intensity of our porous epitaxial Si-C is about seventy times greater than that from the $Al_{.30}Ga_{.70}As$. A similar comparison was performed for one of our strongest porous Si samples which was etched under similar conditions as the porous Si-C sample. Comparison of the porous Si spectrum with $Al_{.30}Ga_{.70}As$, indicates that the intensity from the porous Si sample is a factor of five stronger than that from $Al_{.30}Ga_{.70}As$ as shown in Figure 22b. The latter PL spectra were obtained after photoexcitation with an argon laser at 488 nm at 100 mW.

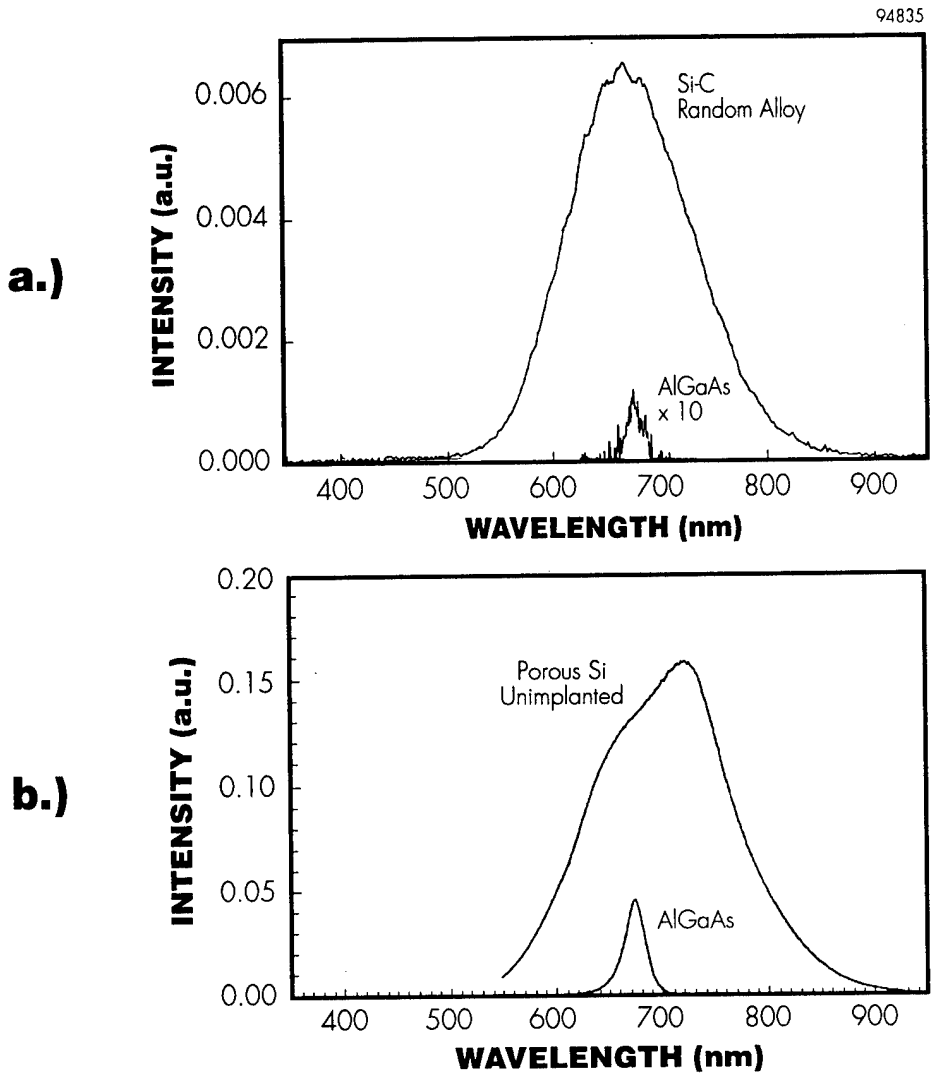


Figure 22 *PL spectra from a) a Si-C porous structure fabricated from anodically-etched epitaxial Si-C and an $Al_{.30}Ga_{.70}As$ sample and b) a porous Si structure etched under similar conditions as 14a and an $Al_{.30}Ga_{.70}As$ sample.*

In addition to studying visible emission from these samples we also studied infrared emission as a function of temperature. Figure 23 shows typical infrared PL spectra at room temperature, 200K, 100K and 9K, which demonstrates the presence of three major peaks at 1440 nm, 1300 nm and 1100 nm. Figure 24 shows temperature vs intensity of the sample in Figure 23. As shown in Figure 24 at room temperature we observed a peak at 1440 nm which rapidly decreased as a function of temperature and completely disappeared at 77K. The second peak was observed at 1300 nm which was very weak at room temperature and was observable at 250K, its intensity then decreased as the temperature decreased and was smallest at 77K. However, from 77K to 9K the peak intensity rapidly increased. The third peak occurred at approximately 1100 nm which was not observable at room temperature, its intensity increased for decreasing temperature until 77K. From 77K to 9K the intensity increased rapidly.

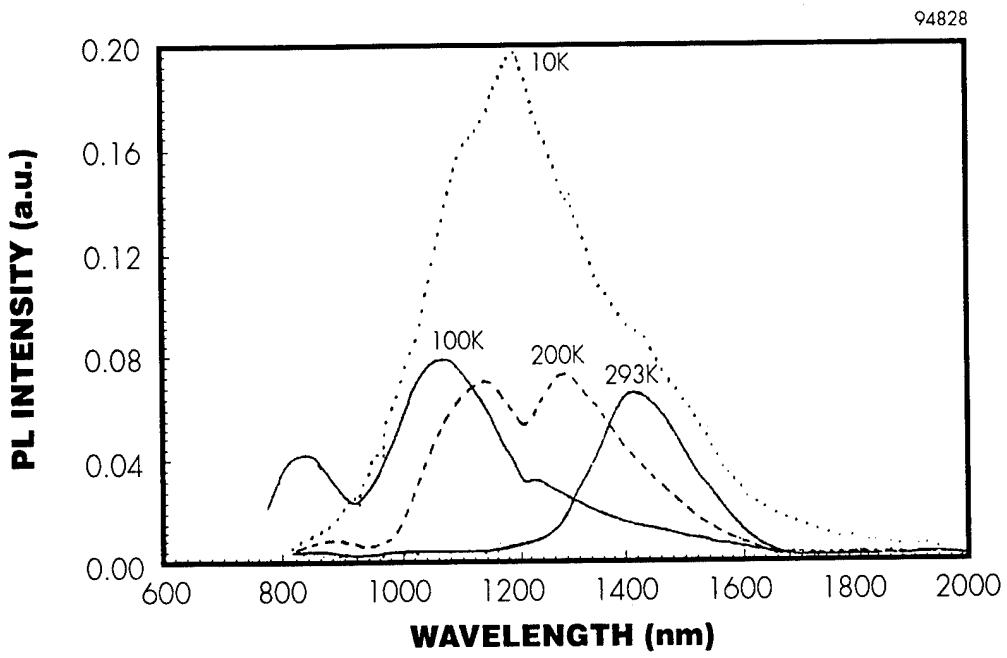


Figure 23 *IR PL spectra of an epitaxially grown Si-C sample, at different temperatures, indicating peaks at 1440 nm, 1300 nm and 1100 nm.*

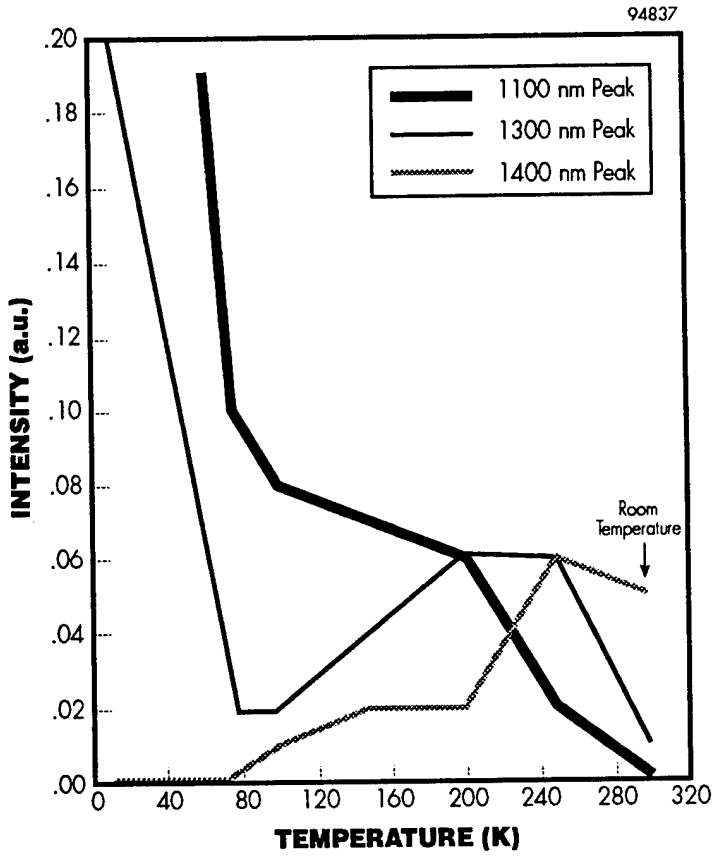


Figure 24 *PL intensity as a function of temperature for a porous structure fabricated on C-doped epitaxial Si.*

4.3.4 Green-blue Emission From Carbon-implanted Porous Si

One method to obtain blue-green emission from porous structures is to transform Si nanostructures which emit red light into Si carbide nanostructures which may emit blue-green light. This basic method involves using carbon implantation and annealing to form a SiC phase. However, one should first develop a recipe to form a SiC phase in bulk Si using the implantation method. Such a process has recently been developed by the PI. However, depending on implantation and annealing conditions, one may obtain poly- or single-crystal SiC structures.

Bulk Si samples which were implanted with a total dose of 1.4 x 10^{18} C/cm^2 were studied by FTIR at NREL by Dr John Webb. Figure 25 shows an infrared transmission spectrum for a SiC thin film (verified by electron diffraction) formed by carbon implantation and annealing. The absorption line at 829 cm^{-1} is similar to that observed from SiC material[66] and the line from about 600 cm^{-1} is typically observed from carbon impurities in Si.[67]

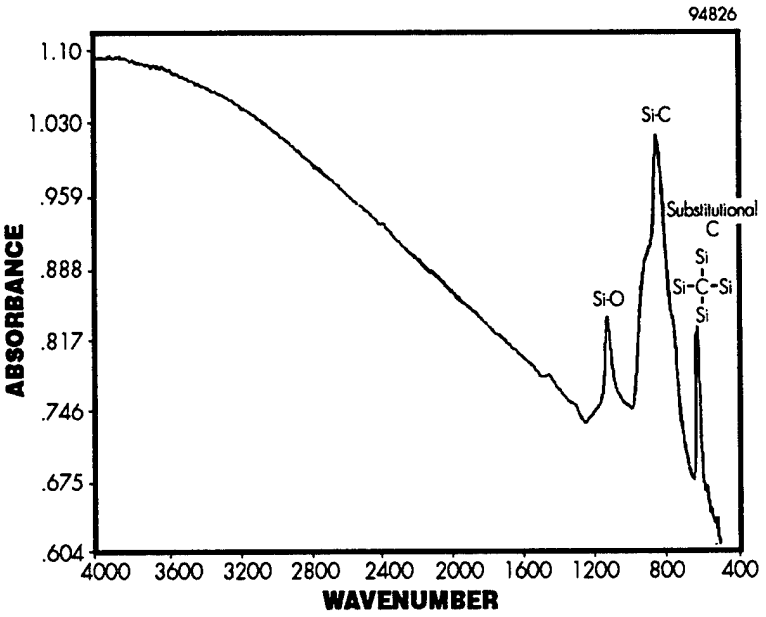


Figure 25 *FTIR spectrum from a thin film SiC layer formed by carbon implantation and annealing of a Si substrate.*

Figure 26 compares PL spectra from a porous Si sample before and after carbon implantation. Typically carbon implantation resulted in a reduction in the PL intensity. Samples were then annealed in N_2 at temperatures ranging from 650 to 1000°C for about 30 to 60 minutes, however, no blue-green light emission was observed. On the other hand, once samples were annealed at 1300°C a strong blue-green PL could be observed with the naked eye. Figure 27 shows photoluminescence results of a porous Si sample which was implanted with a dose of 1 x 10^{16} C/cm^2 at 100 keV. Both the unimplanted and unannealed C-implanted samples were excited at 488 nm at 100 mW. The annealed sample was excited with a UV laser at 325 nm at 9 mW of power. The intensity of these samples were normalized to the same height for comparison. From several samples we studied, this sample (Figure 27) had the strongest blue

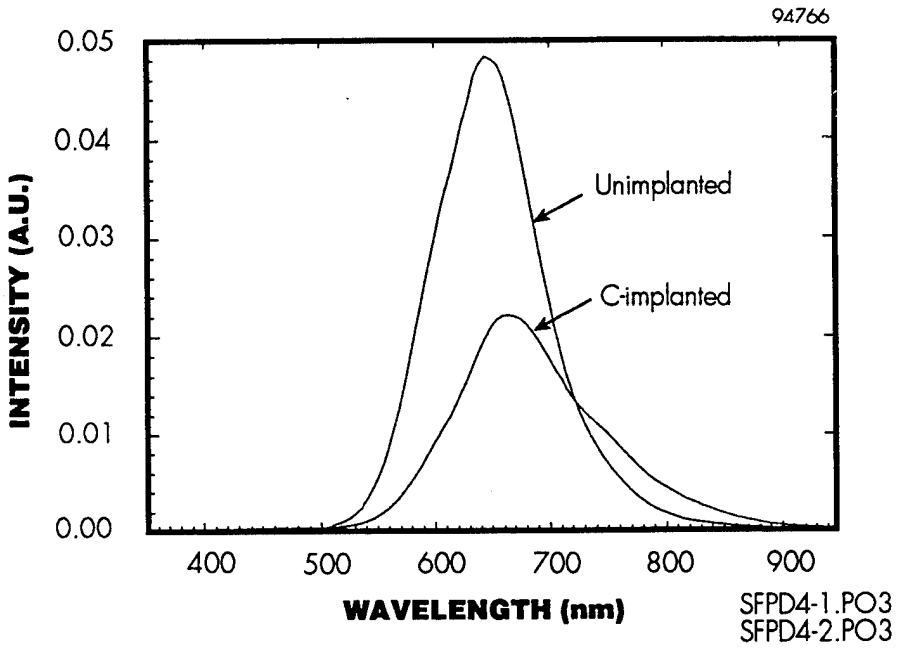


Figure 26 *Visible photoluminescence from a porous Si sample before and after carbon implantation.*

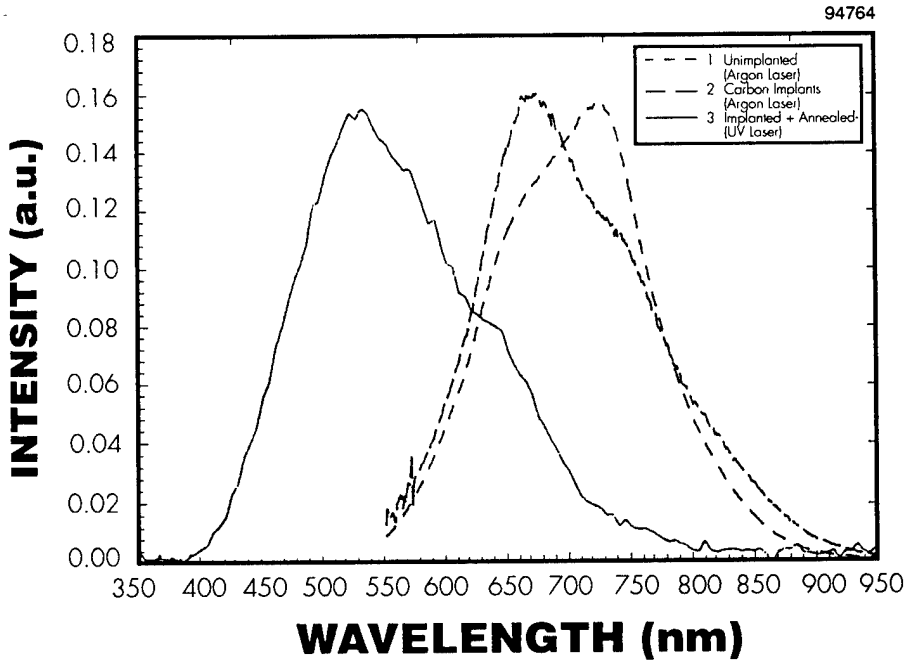


Figure 27 *Normalized spectra of visible PL from a porous Si sample before implantation, after implantation, and after implantation and annealing at 1300°C. These spectra indicate a transformation from a red-emitting porous structure to a blue-green emitting structure.*

emission. Figure 28 compares spectra from a carbon-implanted and annealed sample with an $Al_{.30}Ga_{.70}As$ reference sample and indicates that the green-blue emission from the carbon-implanted porous Si is 20 times stronger than the $Al_{.30}Ga_{.70}As$ sample. Comparing the intensity from an unimplanted porous Si sample with an $Al_{.30}Ga_{.70}As$ sample (Figure 22b) shows that the intensity of the red emission is a factor of 4 stronger than the $Al_{.30}Ga_{.70}As$.

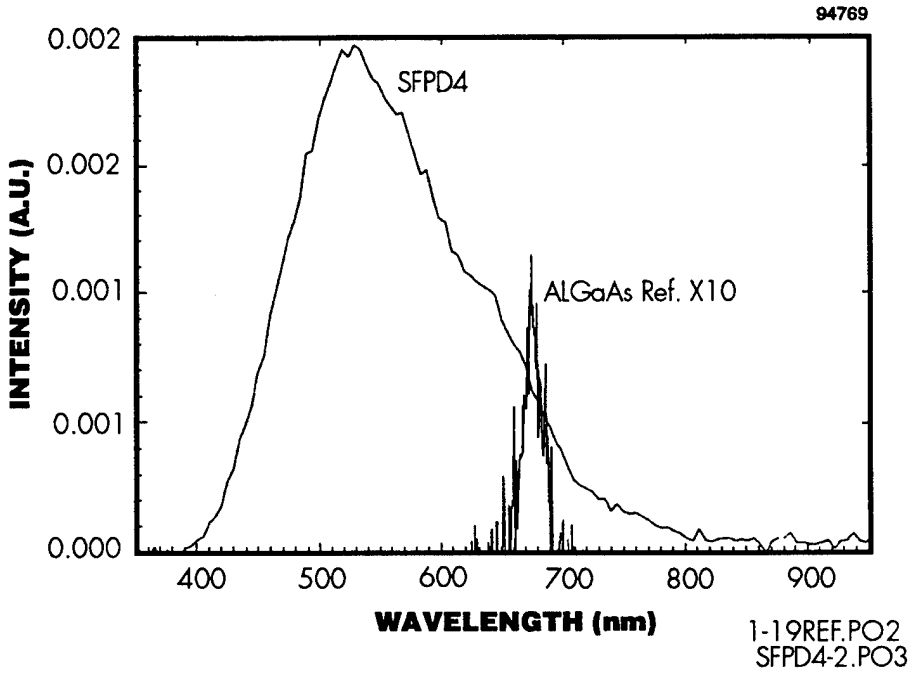


Figure 28 *PL spectra from C-implanted porous Si and an $Al_{.30}Ga_{.70}As$ reference sample; both samples were excited with a UV laser at 325 nm and 9 mW of power.*

We have implanted several samples with carbon using a variety of doses. Typical PL results of a sample implanted with a higher dose (1×10^{17} C/cm^2) are shown in Figure 29. The unimplanted spectra was obtained using an argon laser at 488 nm, while the C-implanted and annealed spectra was obtained using a 325 nm UV laser. For the sample whose PL is shown in Figure 29 the relative intensity of blue-green emission as compared to emission from the unimplanted sample was much lower than the sample which was implanted with a dose of 1×10^{16} C/cm^2. Not all C-implanted and annealed samples had blue emission as emission appears to be dependent on the sample history e.g. etching and implantation conditions.

A paper published by T. Matsumato *et al.*, reported blue-green luminescence from anodically-etched SiC . To fabricate their porous SiC they have used 6H-SiC type single crystal with an indirect bandgap of 2.86 eV (our SiC material has a bandgap of 2.2 eV).[68] Our porous SiC results are very comparable. Nonetheless, our work has a significant advantage because it can be integrated into advanced Si-based technology. Using our technique, the porous Si material (compatible with Si circuitry) can be selectively implanted with carbon to achieve blue emission. Annealing of our material is very important and could eventually be performed by simple laser annealing.

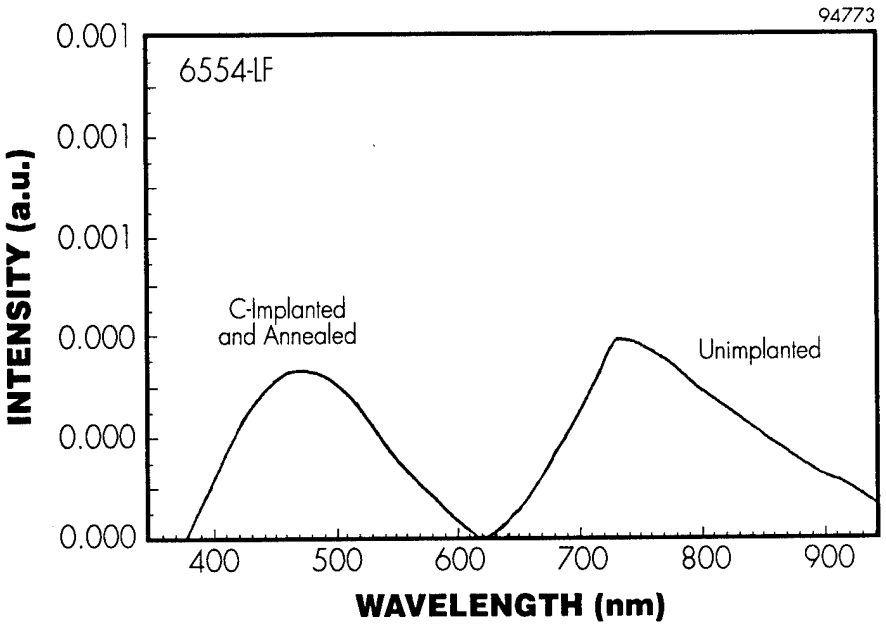


Figure 29 *PL spectra from a porous Si sample before implantation, and after C-implantation with a dose of 1 x 10^{17} C/cm^2 and annealed at 1300°C. Note that the unimplanted spectra was excited with an argon laser at 488 nm and 100 mW, and the implanted spectra was excited with a UV laser at 325 nm and 9 mW.*

FTIR spectroscopy of a carbon-implanted porous Si sample which emits green-blue light (Figure 30) shows the presence of an absorption line at 829 cm^{-1} which is usually seen for SiC. Based on the above data we may deduce that green-blue emission is from SiC with quantum confined properties.

This section demonstrated for the first time a strong, stable blue-green emission from C-implanted red-emitting porous silicon. Porous Si structures fabricated on epitaxially-grown Si-C random alloys showed a 1 to 2 order of magnitude increase in the intensity of red light emission compared to that from porous Si fabricated on non-epitaxial Si. The epitaxially-grown Si-C samples exhibited a strong room-temperature infrared emission at 1440 nm which makes them suitable for infrared LEDs. However, a significant blue shift was observed after carbon implantation into red-emitting porous Si (non-epitaxial) substrates. This green-blue emission was observable by the naked eye. Using AlGaAs as a reference, we observed that the intensity of the green-blue emission was much higher than that of the original red-emitting porous Si.

The electron diffraction pattern of C-implanted and annealed bulk Si has confirmed the formation of β-SiC, which has a bandgap of 2.2 eV. Fourier transform infrared (FTIR) spectra of green-blue emitting porous structures shows infrared absorption lines identical to that of SiC. Based on our experimental data from (a) the electron diffraction patterns of SiC in bulk Si, (b) infrared absorption lines from SiC and from C-implanted porous Si, and (c) green-blue emission from C-implanted porous Si; we conclude that we have formed SiC nanostructures with quantum-confined properties.

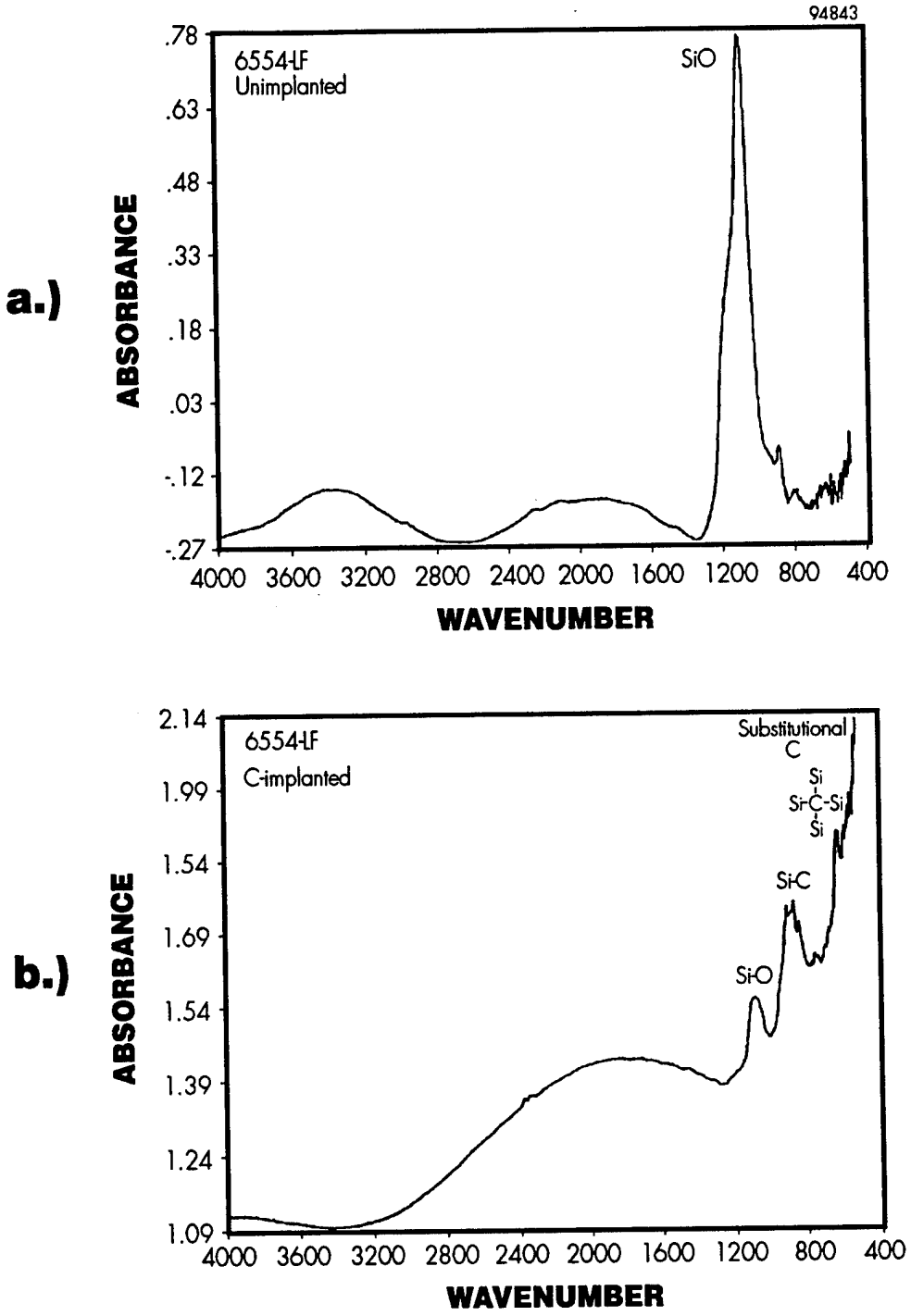


Figure 30 *FTIR spectra of a) red-emitting porous Si and b) C-implanted and annealed green-blue-emitting porous Si with an absorption line which is identical to that reported for SiC.*

4.4 Compatibility of Porous Silicon device Fabrication with Bulk Si Technology

The key to the success of the research on porous Si-based devices lies in the anticipated compatibility of their fabrication processing with bulk Si electronics technology. This compatibility may enable true wafer-scale integration of electronic and optoelectronic devices on the same Si substrate. To accomplish this integration, a patterning process should be developed in order to form porous Si layers only in the selected regions on the wafer. Doan and Sailor have demonstrated photolithographic fabrication of porous Si layers, with etch resolution in order of 20 μm, by projecting a high contrast image onto the Si wafer during the anodic etching.[8] However, this method may be inadequate in true wafer scale integration, as well as being relatively unconventional and with insufficient etch resolution. In true Si wafer-scale integration, because the porous Si surfaces are relatively fragile and the porous Si-based EL devices require relatively low temperature (below 200°C) processes after the formation of the porous layer, these devices should be fabricated after fabricating the Si electronics, which require higher temperature processes. Therefore, development of a simple Si-compatible patterning and masking procedure, by which selected Si areas can be made porous while the existing electronic device regions are protected from reacting with the HF electrolyte, becomes a very important requirement.

This section discusses the development of a series of conventional Si-based photolithographic processing steps used to pattern selected device regions, with resolution better than 5 μm, both before and after the formation of porous Si layers. Additionally, the first true wafer-scale integration using this conventional Si technology has been demonstrated, and a porous Si-based visible-emitting LED and a Si-based photodetector have been processed monolithically on a single Si wafer.

A large number of p- and n-type three-inch Si(100) wafers (with resistivities of about 0.3 ohm-cm) were patterned using conventional photolithography. The wafers were then anodized in an (1:1- HF:ethanol) solution to form luminescent porous Si layers only in selected areas. Positive photoresist (PR) was spun on the wafers, either in single or multiple steps, and cured (soft- and hard-bake) at 90°C for varying periods of time.

Following the formation of selected-area porous Si regions on the p-type substrate, a layer of ITO, about 1500Å thick, was deposited using rf sputtering. The ITO layer was patterned using standard photolithography and etching steps, in order to fabricate isolated ITO/PSL and ITO/Si structures on the same wafer.

Figure 31 shows the photolithographic steps used to pattern Si wafers for subsequent selected-area anodic etching in order to form porous Si, as well as the steps for patterning of the ITO layer.

4.4.1 Patterning of Si Wafers for Selected-Area Anodic Etching

The etch resolution and PL intensity are strongly dependent on both patterning and anodization process parameters. Figures 32a-32c show 200x magnified photographs from three representative samples (P-16, P-20, and P-27) with different etch resolutions. Figure 32d is a photograph of the photomask pattern used in this study. The etch resolution was determined by estimating the variations between the etched and the photomask patterns.

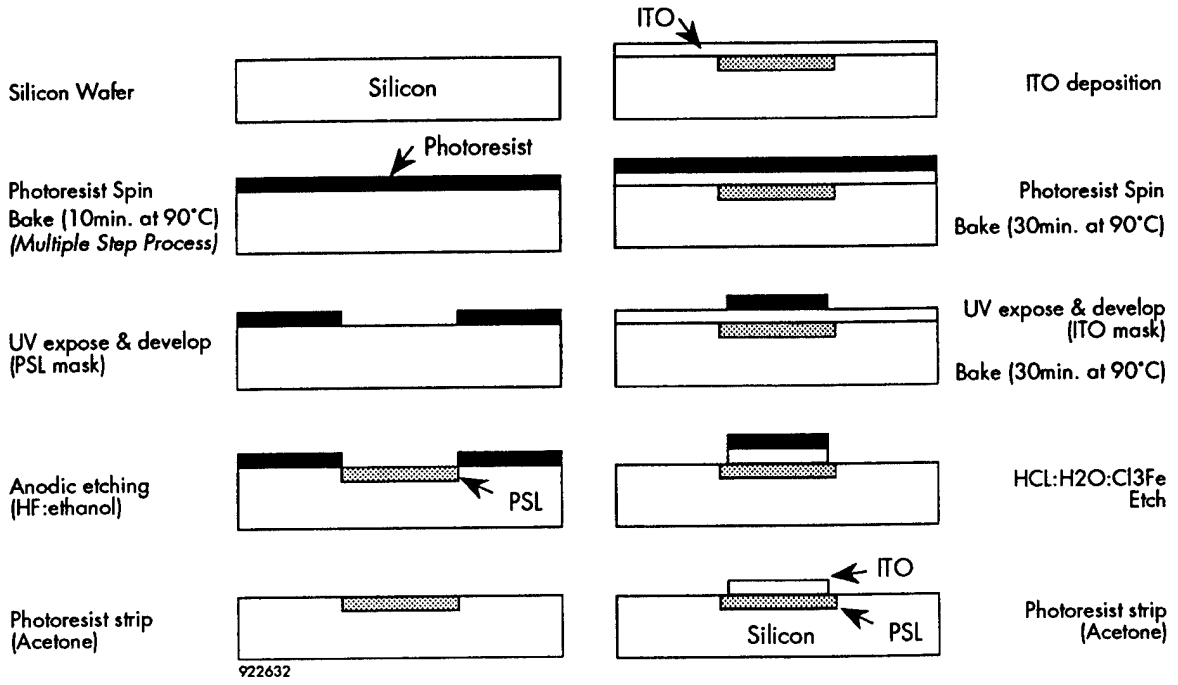


Figure 31 *Processing steps for fabricating PSL/ITO heterojunction LEDs.*

Sample P-16 was patterned using a standard photolithographic process and then anodized for 30 minutes at an applied current of 100 mA. Application of a single photoresist coating followed by a) 30 minute soft-bake (s-bake) at 90°C, b) exposure of pattern, c) development of pattern, and, finally, d) 30 minute hard-bake (h-bake) at 90°C, has been considered the standard photolithographic approach. As shown, this sample's etch resolution in the micrometer-scale is very poor and implies that the photoresist did not provide adequate protection for the adjacent Si regions during the dynamic anodic etching process. In addition, studying larger scale (entire wafer) revealed regions which had been anodized with area sizes on the order of several mm^2. These problems seemed to have been caused by poor adhesion of the PR to the porous Si surface during anodization, as well as localized weakness or defects (such as cracks or pinholes) in the photoresist. The etch resolution appeared to improve for samples which were coated with three layers of PR, with short (10 minutes) soft bake after each PR application (Figure 32b). In addition, the multiple PR coating approach achieved much better etch uniformity across the entire wafer. This uniformity is likely due to the reduced probability for existence of cracks or pinholes in the multiple-resist layers.

The effects of anodic etching parameters on the etch resolution were also studied. Several samples were patterned using the multiple-resist approach and then anodically etched under differing conditions. The etch resolution was significantly improved for samples anodized at lower current densities and for shorter periods of time. Figure 32c (sample P-27) is a photograph of the etch pattern with a resolution of about 4.5 μm on the sample anodically etched at an applied current of 50 mA (about 10 mA/cm^2) for 10 minutes.

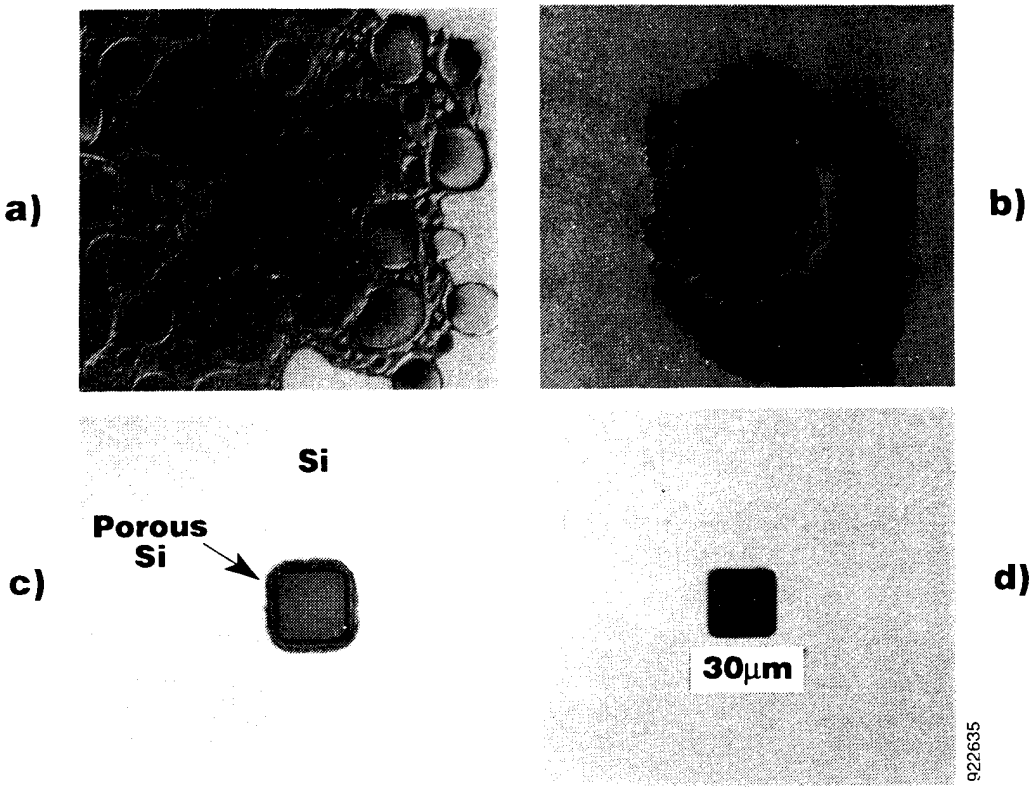


Figure 32 *Microphotographs of a) sample patterned using standard photolithography and anodized at 100 mA for 30 minutes, b) patterned using triple PR-coating process and anodized at 100 mA for 20 minutes, c) sample patterned using triple PR coating process and anodized at 50 mA for 10 minutes, and d) the photomask.*

Figure 33a shows that the etch resolution increases linearly with the anodization current. Due to variations in the etch resolution (etched area) of each sample, accurate values for current density may not be calculated. However, by assuming a value of zero for the etch resolution, the magnitude of current density can be estimated at 4x lower than that of the applied current. From Figure 33b, the relationship between the etch resolution and anodization time for two groups of samples etched at different applied currents also appears to be linear.

PL study of samples in Figures 33a and 33b showed that the PL intensity decreases with lower current densities and reduces the etch time. Therefore, a trade-off seems to exist between the PL intensity and the etch resolution, and one may choose etch procedure based on the application of the porous Si regions. However, no evidence indicates the same trade-off between the etch resolution and the EL intensity in the porous Si-based devices. In fact, our preliminary studies show that EL devices with improved performance may be fabricated using porous Si layers formed at lower anodic current densities and with shorter etch times.

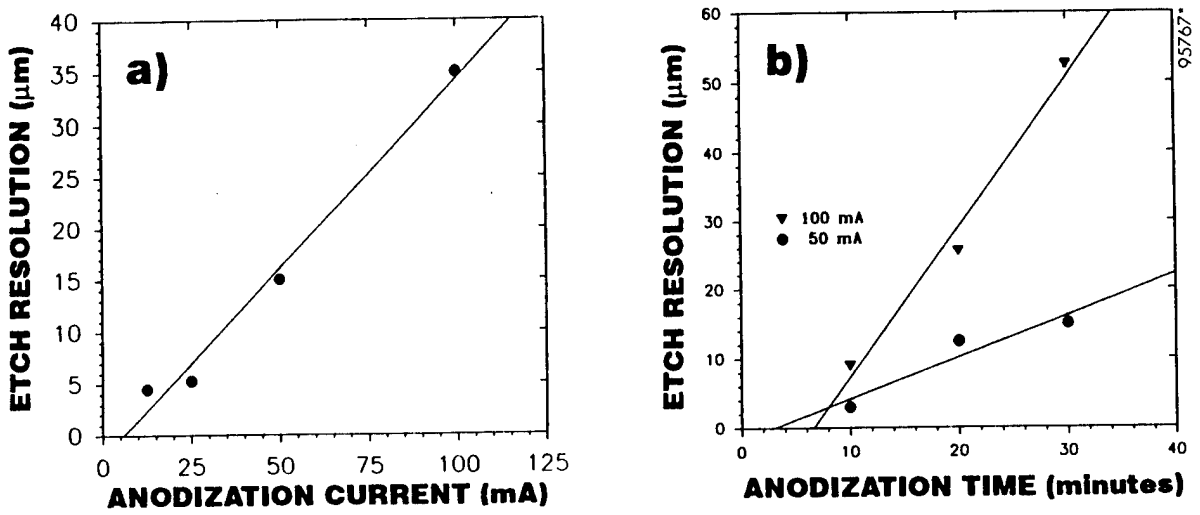


Figure 33 *Effect of a) anodization current and b) anodization time on etch resolution of samples patterned using the multiple resist process.*

4.4.2 Monolithic Processing of Si-Based Optoelectronics (Patterning of ITO Layers)

Monolithic fabrication of photodiodes and visible LEDs on the same Si wafer was demonstrated for the first time by sputter-depositing an ITO layer, about 1500Å thick, on p-type wafers with patterned porous Si layers, followed by a patterning of the ITO layer using standard photolithography and etching off excess ITO in an $HCl:H_2O:Cl_3Fe$ solution. Figure 34a and Figure 34b are photographs of the ITO/Si heterojunction photodiodes (also solar cells) and the ITO/PSL heterojunction LEDs fabricated on the same Si substrate using this approach -- the ITO/Si cells have been fabricated and studied for solar energy conversion applications for a number of years.[9] Figure 35 illustrates the measured current-voltage characteristics and photovoltaic behavior of the ITO/Si photodiodes/solar cells, fabricated monolithically along with the porous LEDs on a single Si wafer.

In this section we have demonstrated that selected-area porous Si regions with pattern resolution better than 5 μm can be formed using conventional photolithographic processes to mask Si wafers during anodic etching in HF electrolyte. The dependence of etch resolution and PL intensity on the photolithographic and anodization process parameters was studied. Monolithic processing of a visible LED and a photodetector on the same Si wafer was demonstrated for the first time. By utilizing proper light transfer media (such as fiber optics, waveguide, or a network of mirrors), optical communication is possible between the Si-based photodiodes and LEDs on the same wafer. Furthermore, a Si-based display panel and its driver circuitry can be fabricated on the same Si substrate.

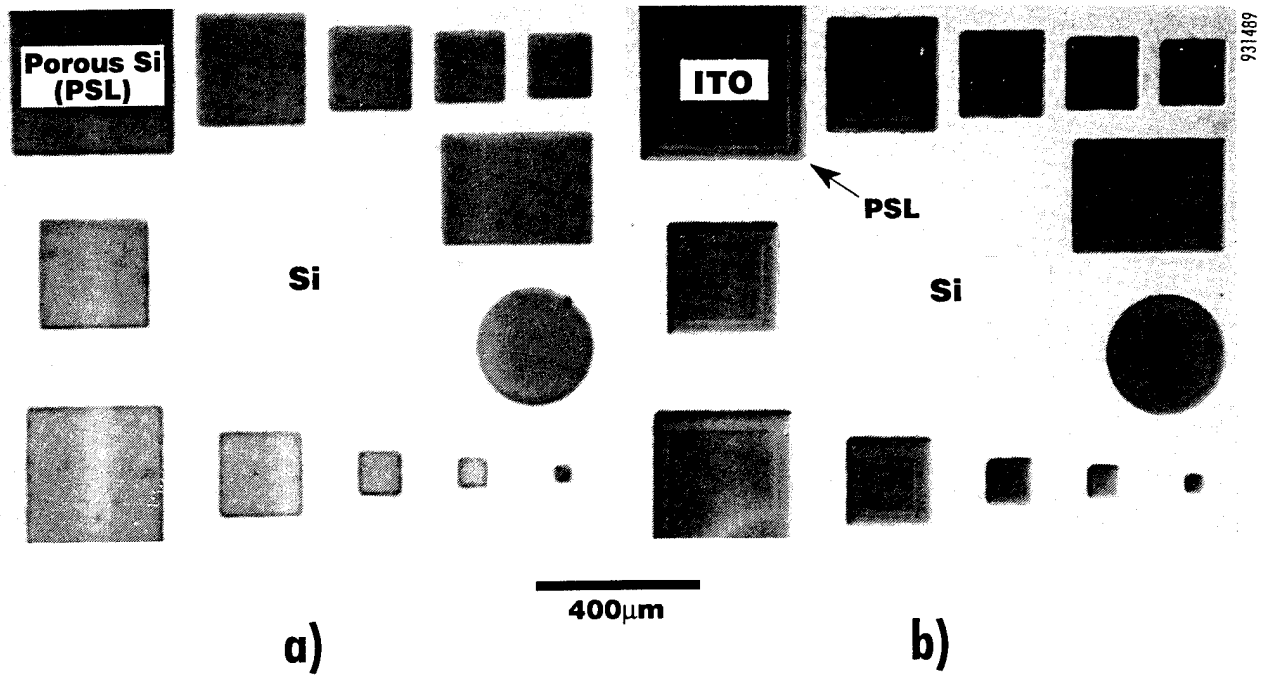


Figure 34 *Microphotographs of a) ITO/Si photodiodes and b) ITO/PSL LEDs fabricated monolithically on a single Si wafer.*

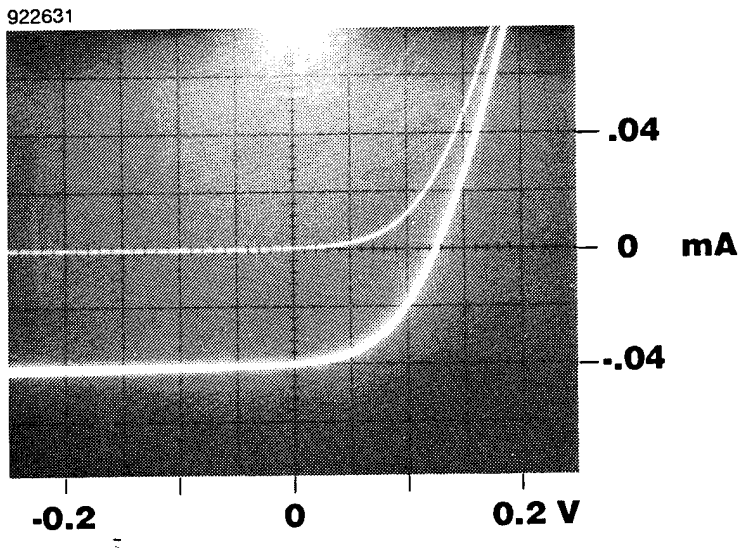


Figure 35 *Current-voltage characteristics of ITO/Si heterojunction photodiodes in dark and under white light illumination.*

4.5 Fabrication of Visible-light-emitting Porous Polycrystalline Silicon Layers

We have investigated the formation of luminescent porous structures on polycrystalline silicon film on glass. Polycrystalline silicon layers are more suitable for large area display applications because they can be deposited readily on glass substrates using conventional techniques such as chemical vapor deposition (CVD).

In addition to thin films, porous layers produced on bulk polycrystalline silicon substrates may also play a significant role in fabricating novel device structures. For example, further advancements in fabricating photovoltaic cells made of porous silicon will make the polycrystalline silicon a logical choice of substrate for mass-producing low-cost porous silicon-based solar cell panels.

In this study, we used commercial photovoltaic-grade bulk polycrystalline silicon substrates produced using the Heat Exchanger Method (HEM™). Control single-crystal substrates were p-type Si(100) wafers with a resistivity of about 0.5Ω-cm. For thin film polycrystalline silicon samples, we used a CVD reactor to deposit 5-10μm of n-type polycrystalline silicon on quartz substrates. After metallization and masking of their back sides, the bulk p-type samples were anodized at room temperature and room light in an electrochemical etching system with a 1(HF):1(ethanol) mixture as the electrolyte. The thin film samples, however, were etched under ultraviolet light illumination, a necessary condition for anodizing n-type Si samples. Current densities ranging from 10-50 mA/cm^2 were applied through the samples for periods between 30 to 105 minutes. A platinum flag was used as the cathode.

Immediately after the formation of porous poly- and single-crystal silicon materials, we used an unfocused 488nm output beam from an argon laser to study the photoluminescence of the samples. Figure 36 compares room temperature PL spectra from p-type porous bulk polycrystalline and p-type bulk single-crystal Si samples anodically-etched for 45 minutes at a current density of about 20 mA/cm^2. As shown, both spectra are similar and both peak at about 650nm (1.9eV) with a FWHM of about 110nm. We noted that the PL intensity from the PPSI sample was higher than that of porous single-crystal Si materials. The stronger PL emission from the PPSI material may be due to the rough original surface of the polycrystalline silicon substrate which has a larger area than standard polished single-crystal Si wafers. However, we also noted that the difference in PL intensity became greater as the etch time increased.

Figures 37a and 37b compare the optical micrographs from the surface of the polycrystalline silicon samples before and after anodic etching. The results in Figure 37b clearly show the porous surface morphology of the sample after anodization. Study of the surface morphology at higher magnifications using scanning electron microscopy (SEM) (Figures 38a and 38b) indicates a faster etch at grain boundaries. As shown, the lateral etch results in the broadening of grain boundaries and the formation of a beveled region from the edge to the center of the boundaries.

We also investigated the light emission from porous materials formed in thin films of polycrystalline silicon deposited on quartz substrates. Plot (a) in Figure 39 shows the PL spectrum from a thin film of PPSI-on-quartz structure irradiated and measured from the front side (polycrystalline silicon) of the sample. Plot (b) in Figure 39, on the other hand, shows the PL

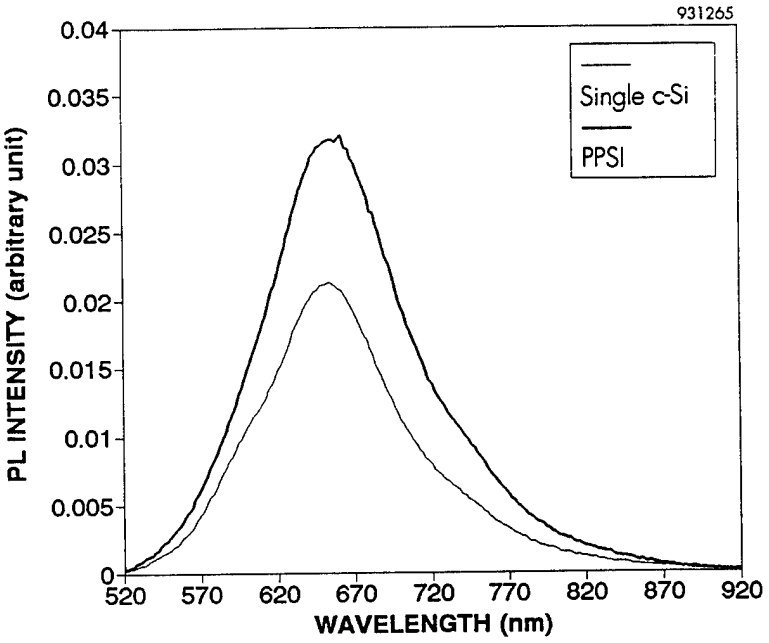


Figure 36 *Comparison of room temperature PL spectra obtained from bulk porous polycrystalline and single-crystal samples produced by anodic etching for 45 minutes at a current density of about 20 mA/cm^2.*

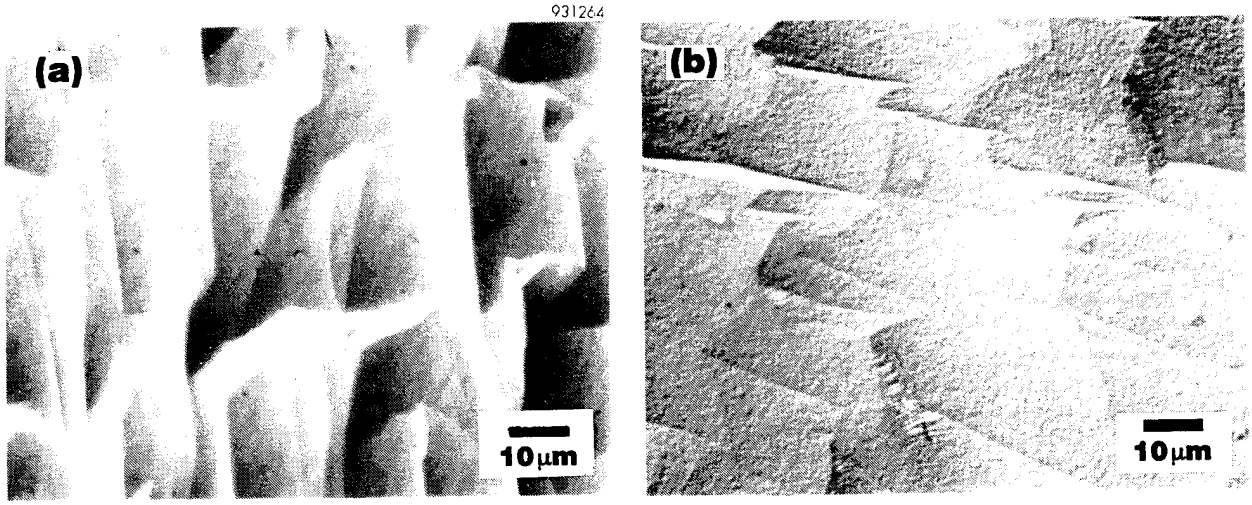


Figure 37 *Comparison between optical micrographs from the surface of the polycrystalline silicon samples: a) before anodic etching and b) after anodic etching.*

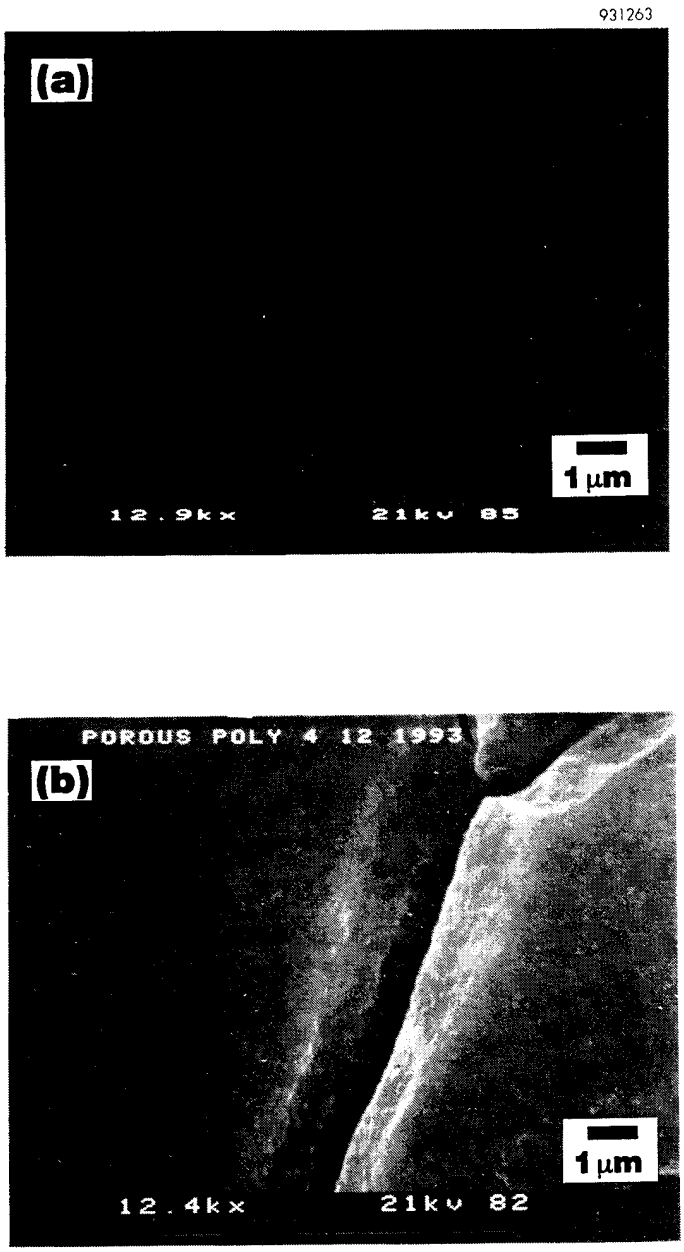


Figure 38 *SEM micrographs of polycrystalline silicon samples: a) before and b) after anodic etching. Note the beveled region micrograph (b) at the grain boundary, indicating a fast etch in both vertical and lateral directions.*

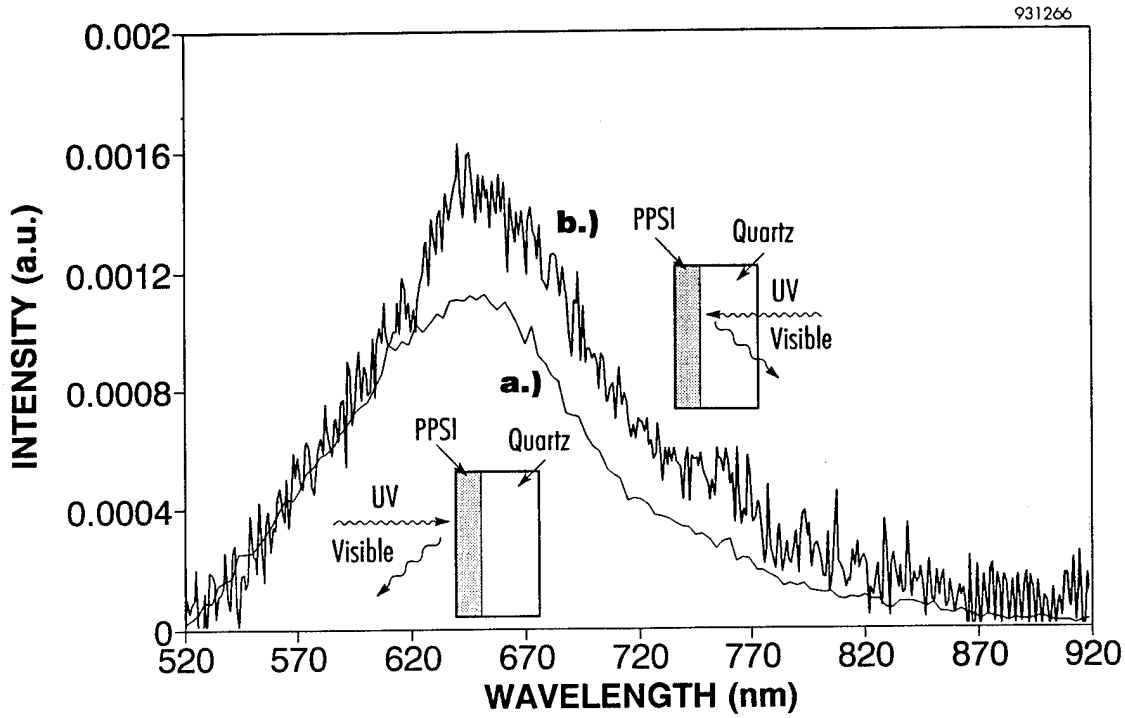


Figure 39 *PL spectrum from thin film of PPSI on quartz: a) irradiated and measured from the front of the sample and b) irradiated from the back of the sample with light emitted through the quartz layer.*

spectrum when the sample was irradiated from the back side (quartz) and the light emitted through the quartz layer. As shown, the spectra measured from either side of the sample are similar with comparable PL intensity. Although we do not fully understand the origin of the fluctuations (noise) in the PL spectrum in Plot (39b), we speculate that they may be due to optical disturbances in the excitation beam (or emitted light) while passing through the quartz substrate. The similarity in the PL spectra of Figures 38 and 39 suggest that the nanostructures formed in the porous n-type polycrystalline Si thin film and those present in the porous p-type bulk samples have nearly the same quantum dimensions.

PL results are very encouraging because they suggest that a thin film of luminescent PPSI material may be used to fabricate devices capable of emitting light through a glass substrate, as in thin-film electroluminescent (TFEL) flat-panel displays. Because these devices would be fabricated on a transparent substrate, the need for a transparent metal contact to the front side of the porous layer would be eliminated. Figures 40a and 40b illustrate typical structures which may be used to fabricate a PPSI-based display device. In the structure of Figure 40a, a thick or thin gold layer may be deposited on a p-type PPSI layer to form a Schottky light-emitting device. Similarly, a pn junction structure with PPSI layers may also be used to produce electroluminescence (Figure 40b).

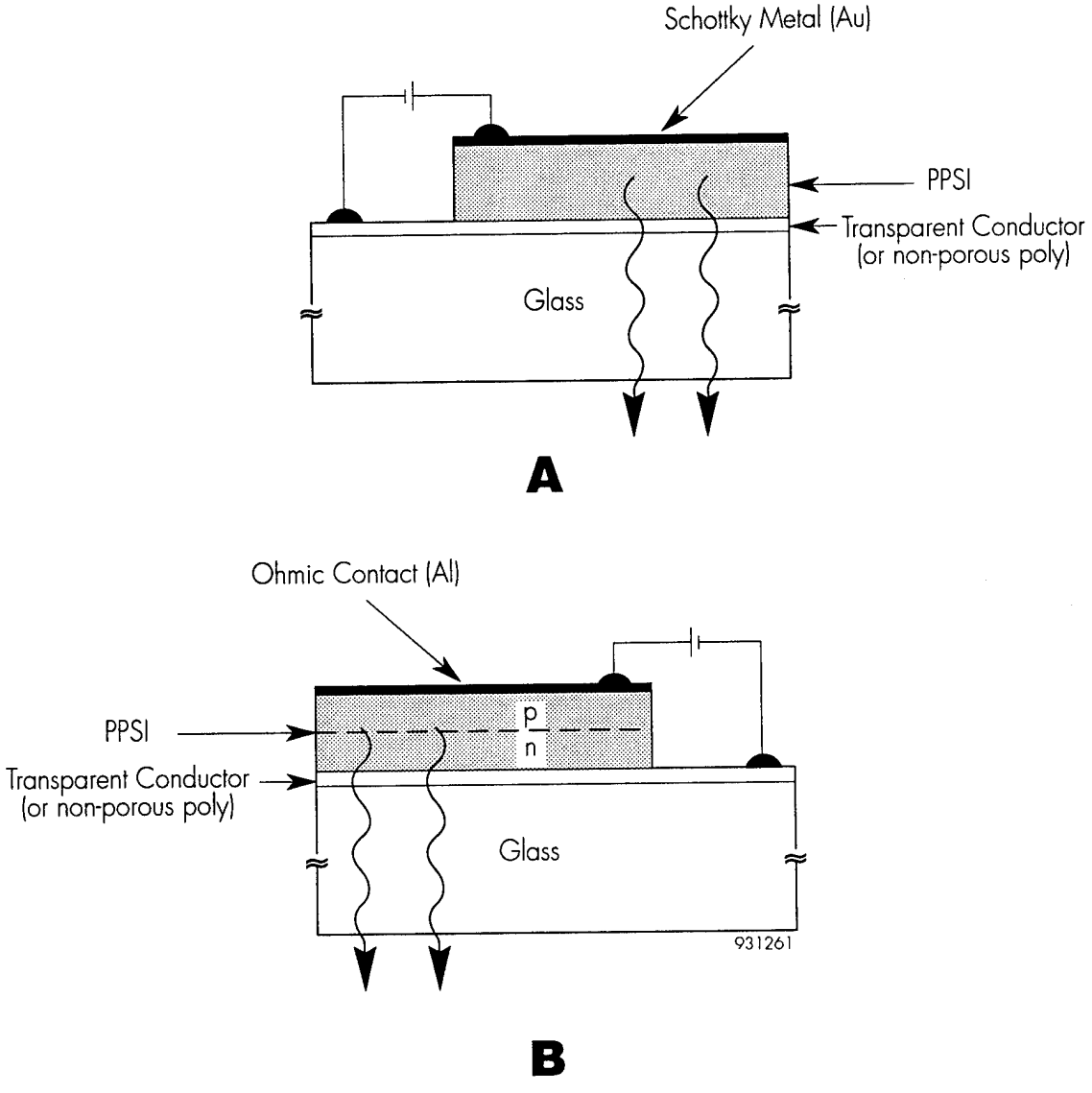


Figure 40 *Typical structures for fabricating PPSI display devices: a) thick or thin gold layer deposited on p-type PPSI layer to form Schottky LED and b) pn junction structure with PPSI layers to produce EL.*

In summary, we produced luminescent nanostructures by anodic etching both bulk polycrystalline silicon wafers and polycrystalline silicon thin films deposited on quartz substrates. Visible light-emitting polycrystalline silicon films offer the possibility of integrating a novel Si-based flat-panel display along with the recently developed TFT driver circuitry on glass substrates. In addition, nanostructures originating from polycrystalline silicon substrates may enable the fabrication of highly efficient photovoltaic cells with very low preparation costs.

5 DISCUSSION AND CONCLUSIONS

5.1 Advantage of Porous Silicon Electroluminescent Devices

The analysis and modeling of porous Si EL devices (LEDs) fabricated at Spire and discussed above have indicated that the observed EL is the result of minority-carrier (electron) injection into the porous Si material. This mechanism is identical to the situation observed with high efficiency GaAs and $Al_{1-x}Ga_xAs$ LEDs. Thus, porous Si LED displays offer a tremendous advantage when compared with traditional high field thin film electroluminescent (TFEL) panels based on ZnS and related II-VI compounds. When using ZnS, a very high voltage (on the order of 100-200 volts) is generally applied, because carrier transport is based on the Fowler-Nordheim emission effect, and is then followed by impact excitation of dopant centers.[69] In porous silicon LEDs, Spire's studies have indicated that EL is related to band-to-band recombination between quantum-confined energy levels located in the conduction and valence bands of the material; it is not restricted by low level concentration of dopants such as manganese or rare earths, as in ZnS EL displays. In ZnS devices, the current and the light emission intensity are typically related to the reciprocal of the square root of the applied voltage[70] (Fowler-Nordheim equation).[71] Porous Si LEDs proved to have the brightness directly proportional to the current, with the current depending exponentially on the applied voltage, which is exactly equivalent to GaAs LEDs.[43] Spire's porous Si data failed to fit the Fowler-Nordheim equation over any range of parameters, while exactly fitting Shockley's minority-carrier injection equation.

Because our analysis indicates that no high field impact ionization process is required for the operation of porous silicon LEDs, good PL results should be exactly reflected in good EL results, analogous to GaAs, but in contrast with ZnS. Figure 41 shows several mechanisms of light emission from semiconductors. PL (Figure 41a) involves only a single electron. Incoming light promotes the electron to the empty conduction, and there are negligible electric fields present. In the absence of a field, the electron remains in place until it radiatively recombines into the valence band. Injection EL is very similar, with a negligible electric field in the region of light emission; as shown in Figure 41b, the single electron moves into the recombination by diffusion, and holes are already present in the valence band due to doping. Thus, PL and minority-carrier injection EL are equivalent processes. Alternately, the electroluminescence in TFEL devices is produced either by impact excitation (as shown in Figure 41c for ZnS:Mn) or by impact ionization (as shown in Figure 41d for ZnS:Cu,Cl); both (similar) processes depend on high electric fields. As shown in Figure 41c, impact excitation involves two electrons: the first is accelerated by the field to a very high energy, whereupon it can transfer momentum to a second electron located at a dopant, such as manganese. Return of the second electron to its ground-state causes light emission. Unfortunately, much external energy, more than is gained in the light emission, must be supplied to the device in order to achieve a population of hot electrons. The fourth mechanism, impact ionization, is the least efficient, because now three electrons are involved. The first one is again accelerated to a high energy level and collides with

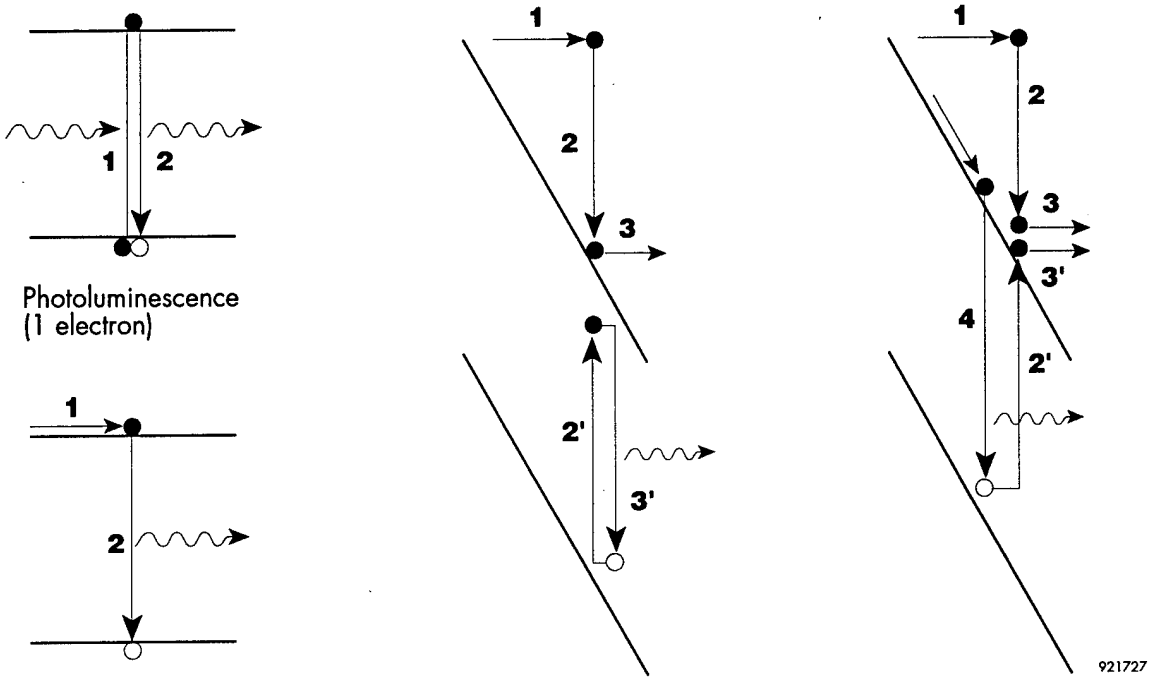


Figure 41 *(a) Mechanism of PL; (b) mechanism of minority-carrier EL; (c) schematic of electron flow in high field impact excitation EL; and (d) schematic of electron flow in high field impact ionization EL.*

an electron located on a filled acceptor level, transferring its momentum. Here, however, the second electron is promoted into the conduction band where the field also pulls it away. Therefore, a third electron must appear to recombine with the stationary hole: In the presence of a high field, this is unlikely. Clearly, in the last two cases, efficient PL does not necessarily correlate with efficient EL because of the presence of the high field during electroluminescence.

As discussed in Section 5.1, interface states at the ITO/porous Si heterojunction resulted in the reduction of light efficiency of active devices. However, the quantum efficiency of present devices has been mostly compromised because the contacting areas between wide bandgap materials (pn devices) or metal contacts (Schottky), and porous Si, are only a very small portion of the total porous Si surface (Figure 42a). Sputtering or e-beam evaporation techniques, used

for LED fabrication, only provide a contact to the tip of the pores (see Figure 42), therefore, most of the surface of the light-emitting porous Si region is inactive in EL. Use of transparent conducting polymers in principal may result in an enhancement in light efficiency. However, at the present time, these devices suffer from a lack of stability. A process which could result in conformal coverage (Figure 42b) of a transparent, conductive wide bandgap material into porous Si might enhance the quantum efficiency to the impressive efficiency levels observed from porous Si with a liquid junction.[7] For example, atomic layer epitaxy (ALE) growth of GaN (side-wall epitaxy),[72] or electroplating of a transparent conducting oxide could increase the contact area which would result in an enhancement of EL efficiency.

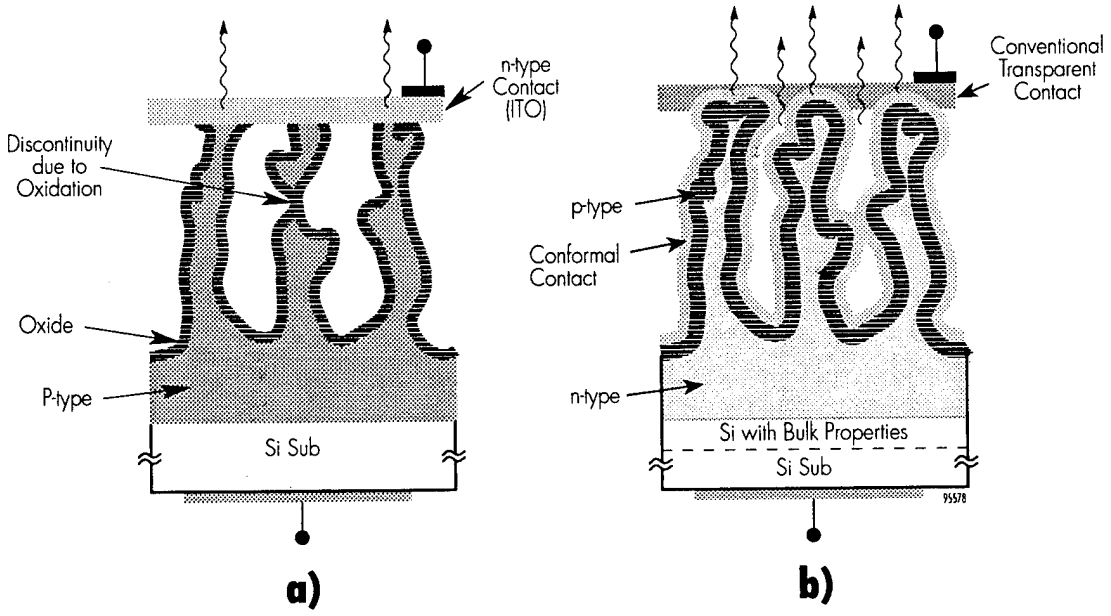


Figure 42 *Comparison of porous Si structures with a) contact layer produced by sputtering or evaporation and b) an idealized structure with a conformal contact which covers the entire porous Si surface.*

Another phenomena which influences the external quantum efficiency of light emitting devices (including porous silicon but to a much lesser degree) is self absorption which is not well understood in porous silicon. Since Si is transparent to wavelengths longer than 1.1 μm, the self absorption or reduction of external quantum efficiency will not be a problem if porous Si is used as a medium for rare earth elements or as a light source for IR emission at wavelengths longer than 1.1 μm. In that case restrictions on the thickness and optical properties of the contact material to the porous region would be relaxed and IR could exit from either side of the wafer. In particular, if the visible light from porous Si is used to pump embedded Er the self absorption would not be a problem.[73]

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APPENDIX A

LIST OF RELEVANT PATENTS, PUBLICATIONS, AND ARTICLES

RELEVANT PATENTS AND INVENTIONS

F. Namavar, N.M. Kalkhoran, and H.P. Maruska, U.S. Patent No. 5,272,355. "Optoelectronic Switching and Display Device and Method," December 21, 1993.

PUBLICATIONS

"Visible Electroluminescence from Porous Silicon np Heterojunction Diodes," F. Namavar, H.P. Maruska, and N.M. Kalkhoran, *Appl. Phys. Lett.* **60** (20), 2514, 1992.

"Current Injection Mechanism for Porous-Silicon Transparent Surface Light-Emitting Diodes," H.P. Maruska, F. Namavar, and N.M. Kalkhoran, *Appl. Phys. Lett.* **61** (11), 1992.

"Energy Bands in Quantum-Confined Silicon Light-Emitting Diodes, "H.P. Maruska, F. Namavar, and N.M. Kalkhoran, *Appl. Phys. Lett.* **63** (1), 5 July 1993.

"Further Evidence for Quantum Confinement in Porous Silicon,"R. Behrensmeier, F. Namavar, G.B. Amisola, F.A. Otter, J.M. Galligan, *Appl. Phys. Lett.* **62**, May 10, 1993.

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